Personal Computer

Service Reference Manual

MultiSpeed

NEC NEC Corporation

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1. System Outline

This manual mainly explains the MultiSpeed hardware features so that MultiSpeed users can figure out the basic concept of its architecture.

1.1 Construction of System Board

The MultiSpeed system unit board is divided into four sections called the main section, memory section, FDC (floppy disk controller) section, and PS (power supply) section, as follows:

- Main section: MultiSpeed's core board which comprises the CPU, timer, interrupt controller, etc.
- Memory section: Board which comprises main RAMs and ROMs
- FDC section: Board which comprises the FDC, DMA controller, etc.
- PC section: Board which supplies necessary power levels.

These four sections PC boards (printed-circuit boards) must all be connected mutually and correctly; otherwise, the MultiSpeed will malfunction. Pin assignment for the connectors which connect these PC boards are described later.

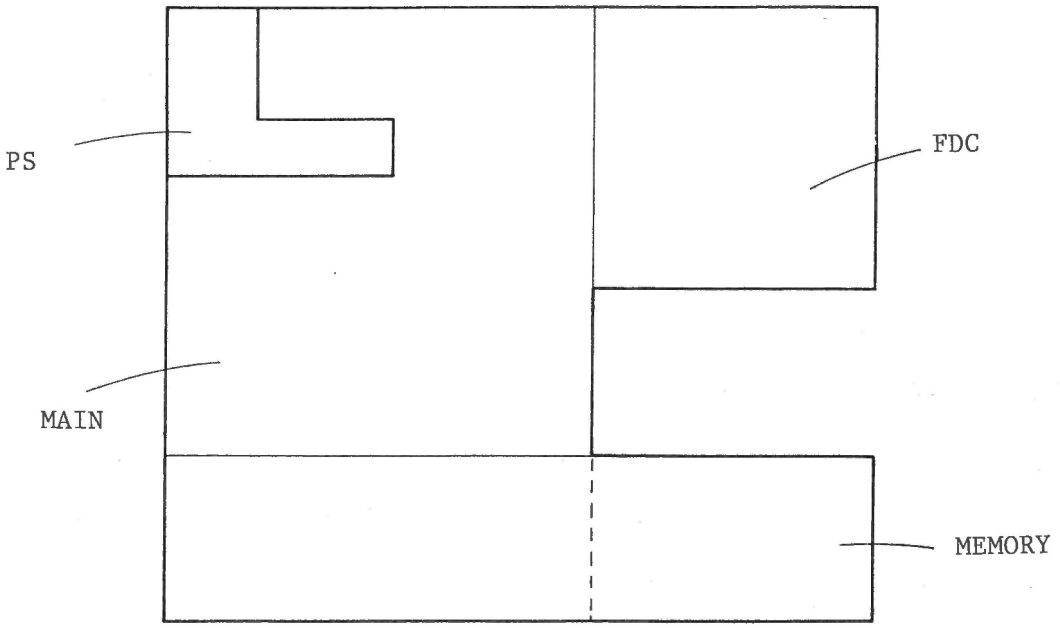
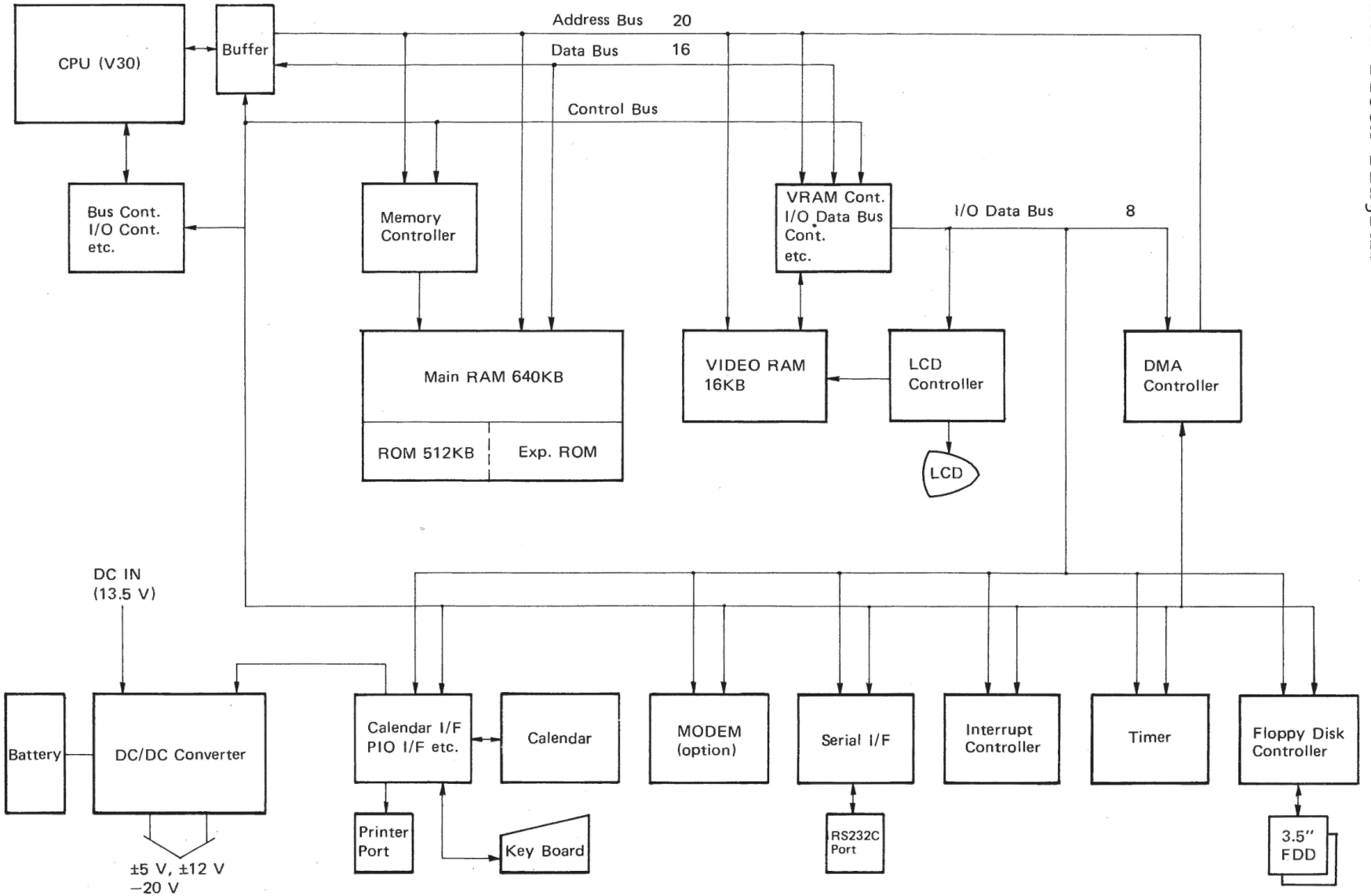
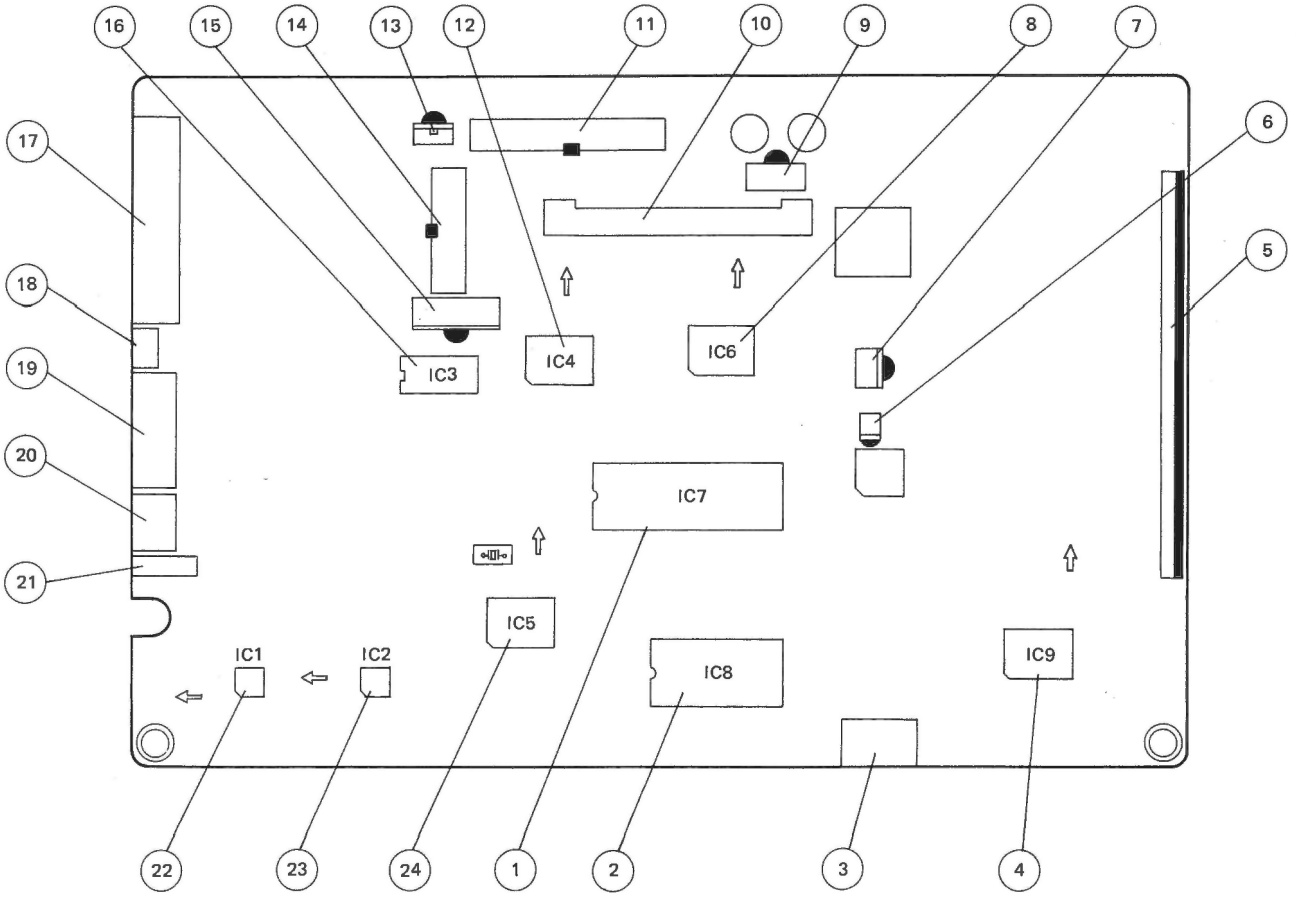


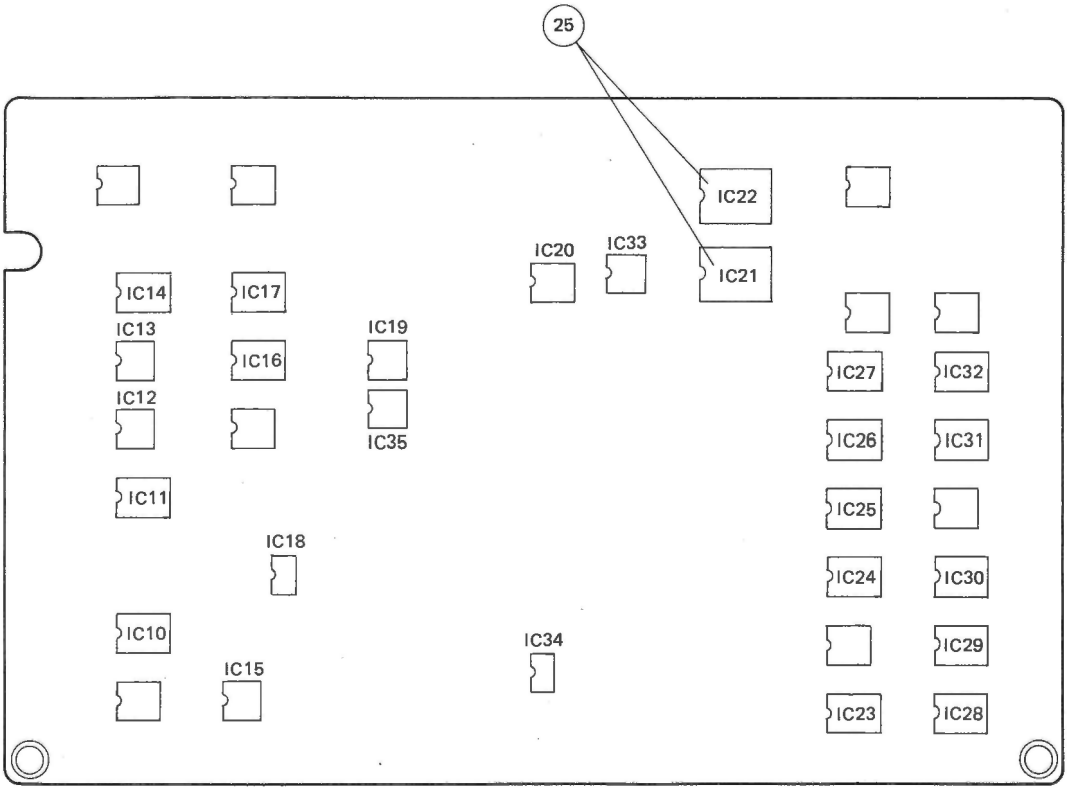
Fig. 1.1 System board layout


CPU (V30)
Buffer
Address Bus 20
Data Bus 16
Control Bus
Bus Cont.
I/O Cont.
etc.
Memory Controller
VRAM Cont.
I/O Data Bus
Cont.
etc.
I/O Data Bus 8
Main RAM 640KB
ROM 512KB
Exp. ROM
VIDEO RAM
16KB
LCD Controller
LCD
DMA Controller
DC IN
(13.5 V)
Battery
DC/DC Converter
±5 V, ±12 V
−20 V
Calendar I/F
PIO I/F etc.
Calendar
Printer Port
Key Board
MODEM
(option)
Serial I/F
RS232C Port
Interrupt Controller
Timer
Floppy Disk Controller
3.5"
FDD

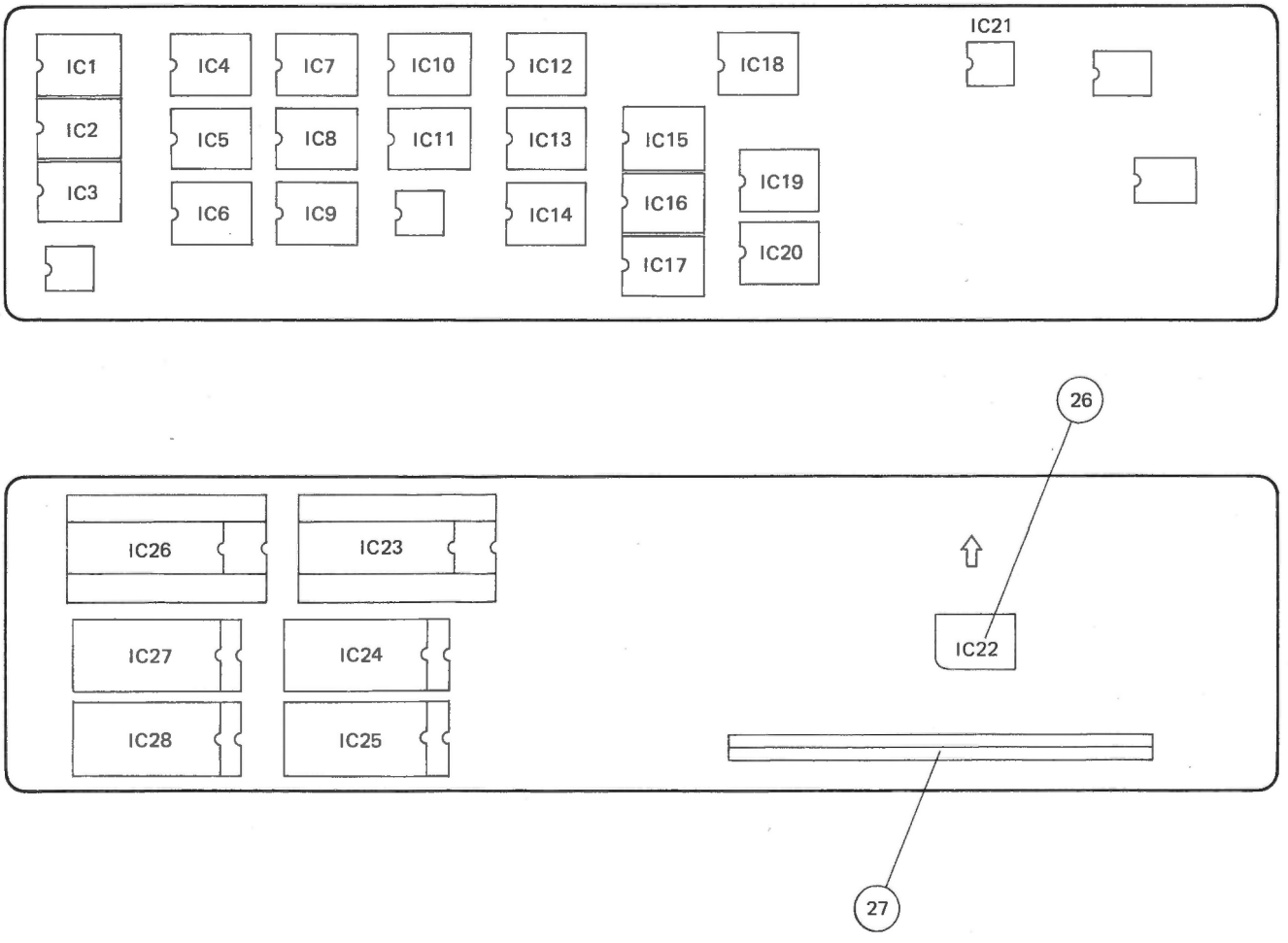
1.3 Parts Layout

1.3.1 MAIN Board

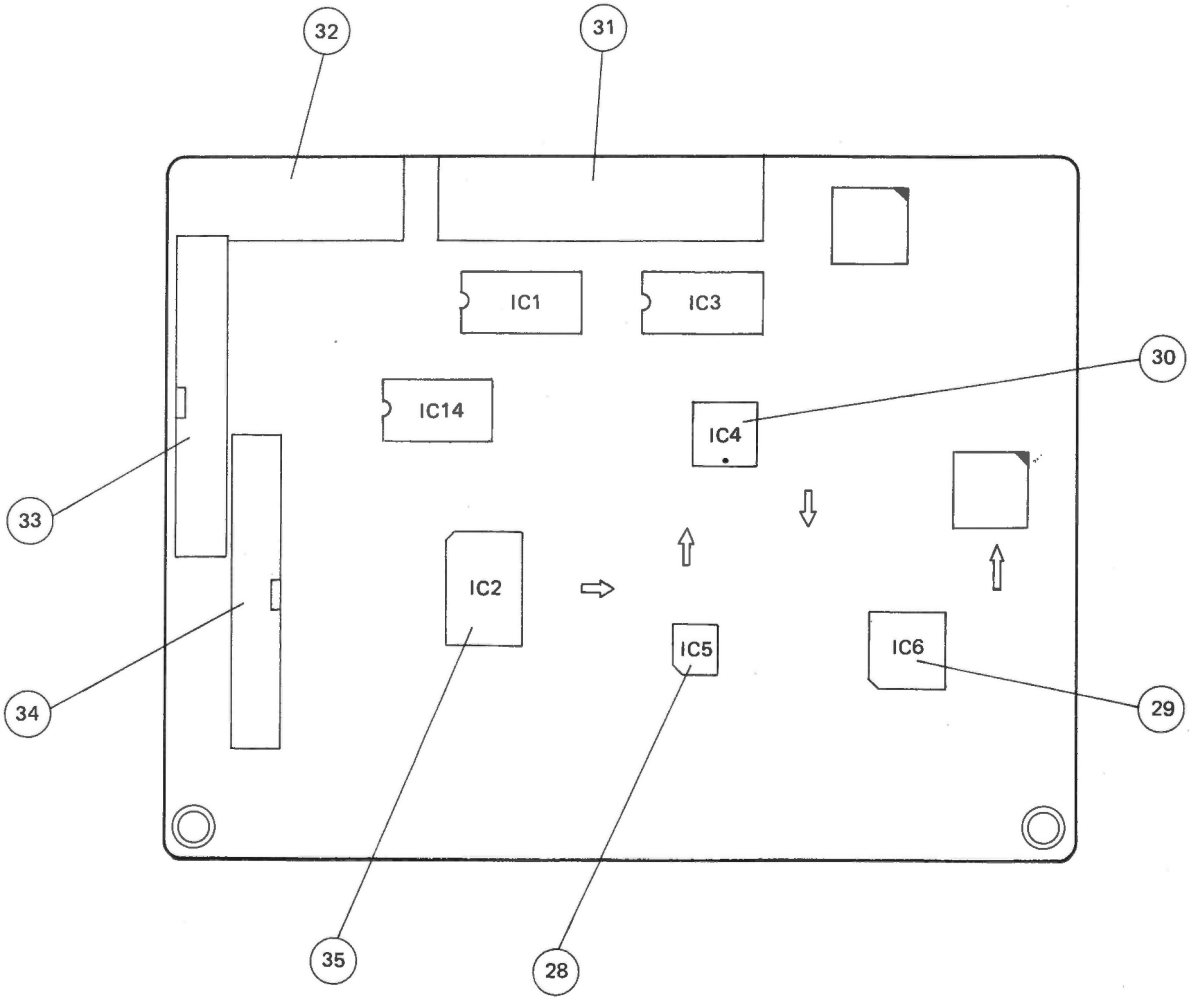


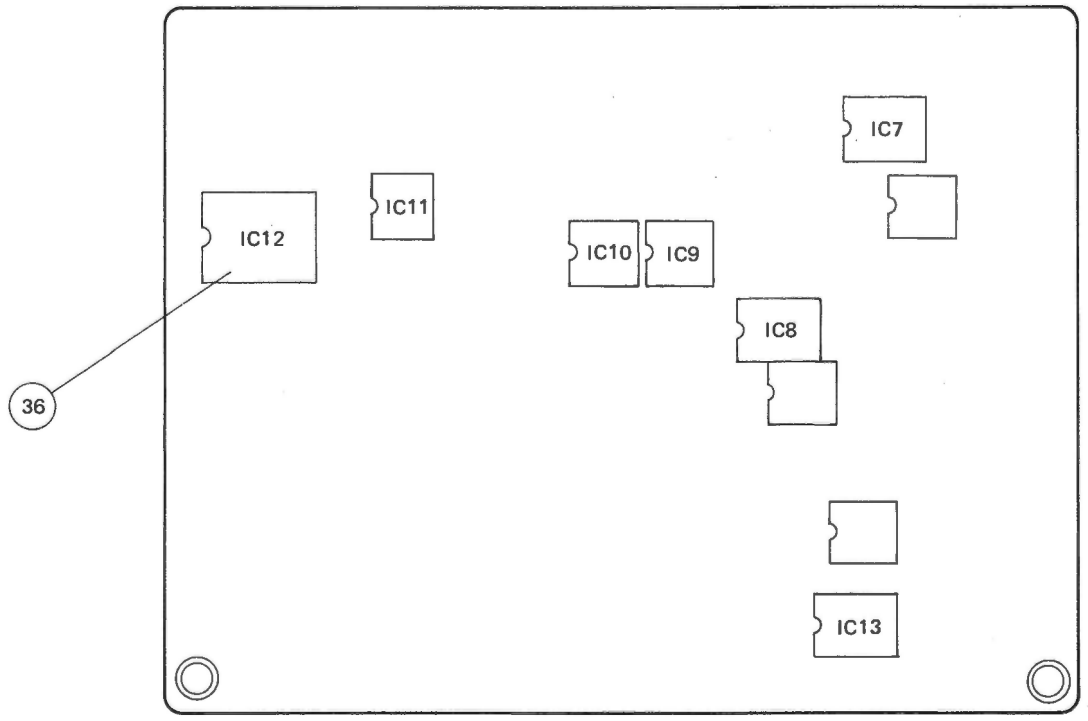


1.3.2 MEMORY Board



1.3.3 FDC Board





1.3.4 List of Parts on Boards*

① Processor μPD70116-10
② Character Generator ROM
③ Power SW
④ GATE ARRAY SLA6170FIJ
⑤ MAIN-MEMORY Connector
⑥ Speaker Connector
⑦ LED Connector
⑧ GATE ARRAY SLA6170FIK
⑨ KEY BOARD Connector
⑩ MODEM Connector
⑪ MAIN-FDC Connector
⑫ GATE ARRAY SLA6170FIL
⑬ FDD POWER Connector
⑭ LCD Panel Connector
⑮ POWER SUPPLY Connector
⑯ Real Time Clock RTC 58321
⑰ PRINTER Connector
⑱ Backup Battery SW
⑲ CRT Connector
⑳ Configuration SW
㉑ RESET SW
㉒ Interrupt Controller μPD71059
㉓ Timer Counter μPD71054
㉔ LCD/CRT Controller V6355
㉕ VRAM
㉖ GATE ARRAY SLA6170FIM
㉗ MAIN-MEMORY Connector
㉘ DMA Controller 82C37-5
㉙ Floppy Disk Controller μPD72065
㉚ Asynchronous Communication Element 82C50
㉛ RS-232C Connector
㉜ EXT-FDC Connector
㉝ FDD Connector
㉞ MAIN-FDC Connector
㉟ GATE ARRAY μPD65013G-096

* The numbers in front of part names correspond to the numbers shown in the figures of 1.3.1 to 1.3.3.

1.4 Pin Assignment of Connectors (MAIN)

* The direction of I/O of each pin is based on the MAIN Board.

1.4.1 LCD Connector

Pin number	Signal name	I/O	Remarks
1	UD0	O	Upper Screen Data 0
2	UD1	O	Upper Screen Data 1
3	UD2	O	Upper screen data 2
4	UD3	O	Upper Screen Data 3
5	ECLK	O	Chip Enable
6	FLMU	O	Upper Screen Frame Signal
7	DF	O	AC Signal for Liquid Cristal
8	LOAD	O	Data Latch
9	CP	O	Data Shift
10	LD0	O	Lower Screen Data 0
11	LD1	O	Lower Screen Data 1
12	LD2	O	Lower Screen Data 2
13	LD3	O	Lower Screen Data 3
14	FLML	O	Lower Screen Frame Signal
15	+5		Power Supply for Logic Drive
16	Vss		Ground
17	-15		Power Supply for Liquid Cristal
18	FG		Frame Ground (connected No.16 Pin)
19	L5	O	Reserved
20	L4	O	Reserved

1.4.2 Key Board Connector

Pin number	Signal name	I/O	Remarks
1	KBD	I/O	Serial Data Line to sub CPU on the Keyboard
2	DI	I/O	DATA Enable
3	RESET	O	Reset to sub CPU
4	GND		Ground
5	+5		Power Supply

1.4.3 Power Connector

Pin number	Signal name	I/O	Remarks
1	GND		Ground
2	-20		Power Supply for LCD
3	-12		Power Supply for RS232C and MODEM
4	+12		Power Supply for RS232C and MODEM
5	-5		Power Supply for MODEM
6	+5		Power Supply for Logic Circuits
7	REMOTE	O	enable PS Board
8	BB CHARGE	I	Power Supply for Backup Battery Charge

1.4.4 FDD Power Connector

Pin number	Signal name	Remarks
1	+5	Power Supply for FDD
2	GND	Ground
3	GND	Ground
4	+5	Power Supply for FDD

1.4.5 SP Connector

Pin number	Signal name	Remarks
1	—	Amplified Audio Output (-)
2	+	Amplified Audio Output (+)

1.4.6 MEMORY PWB Connector

Pin number	Signal name	I/O	Remarks
1	MA1	O	Address Bus for Memory
2	MA2	O	↑
3	MA3	O	↑
4	MA4	O	↑
5	MA5	O	↑
6	MA6	O	↑
7	MA7	O	↑
8	MA8	O	↑
9	MA9	O	↑
10	MA10	O	↑

Pin number	Signal name	I/O	Remarks
11	MA11	O	↑
12	MA12	O	↑
13	MA13	O	↑
14	MA14	O	↑
15	MA15	O	↑
16	UBE	O	Upper Byte Enable (-)
17	A15	O	Address Bus from CPU Directly
18	A16	O	↑
19	A17	O	↑
20	A18	O	↑
21	A19	O	↑
22	A0	O	Address Bit 0 (LSB)
23	ADD16	I	Latched Upper Bus
24	ADD17	I	↑
25	ADD18	I	↑
26	ADD19	I	↑
27	UBEN	I	Latched Upper Byte Enable (-)
28	LBANK0	O	External ROM Bank Select
29	HRA16	O	External ROM Bank Select
30	BANK0	O	inverted BANK SELECT BIT 0 in Port E0h
31	MA16N	O	inverted Memory Address Bit 16
32	MA16	O	Memory Address Bit 16
33	EXRCS1	O	External ROM Chip Select 1
34	EXRCS2	O	External ROM Chip Select 2
35	AEN	O	Address Enable
36	ASTB	O	Address Strobe
37	IOR	O	I/O Read
38	WIOR	I	Wide I/O Read
39	CLKN	O	inverted System Clock
40	MSEL	O	Memory Select
41	OUT1	O	OUT Signal from Timer (for Memory Refresh)
42	DRQ0	O	DMA Request Channel 0 (for Memory Refresh)
43	UMDEN	O	Upper Memory Data Enable
44	LMDEN	O	Lower Memory Data Enable
45	DACK0	I	DMA Acknowledge Channel 0 for Memory Refresh
46	XDEC0	O	ROM Bank #0 Select
47	XDECR	O	ROM Bank #1,#2 Select
48	ADECR	I	Decoded Upper Address
49	WMEMR	I	Wide Memory Read
50	MEMR	O	Memory Read
51	MEMW	O	Memory Write
52	MD0	I/O	Data Bus for Memory
53	MD1	I/O	↑
54	MD2	I/O	↑
55	MD3	I/O	↑
56	MD4	I/O	↑
57	MD5	I/O	↑
58	MD6	I/O	↑
59	MD7	I/O	↑
60	MD8	I/O	↑

Pin number	Signal name	I/O	Remarks
61	MD9	I/O	↑
62	MD10	I/O	↑
63	MD11	I/O	↑
64	MD12	I/O	↑
65	MD13	I/O	↑
66	MD14	I/O	↑
67	MD15	I/O	↑
68	MEMRST	O	Reset to Protect the Data in Backup Memory
69	+5		Power Supply
70	+5		Power Supply
71	+5		Power Supply
72	+5		Power Supply
73	B+5		Power Supply for Memory Backup
74	B+5		Power Supply for Memory Backup
75	GND		Ground
76	GND		Ground
77	GND		Ground
78	GND		Ground
79	NC		
80	NC		

1.4.7 LED Indicator Connector

Pin number	Signal name	Remarks
1	LED1	Floppy Disk Drive A Select indicator
2	LED2	Froppy Disk Drive B Select indicator
3	LED3	Low power indicator
4	+5	Power Supply

1.5 Pin Assignment of Connectors (FDC)

The Direction of I/O of each pin is based on the FDC Board.

1.5.1 FDC PWB Connector

Pin number	Signal name	I/O	Remarks
A1	GND		Ground
A2	GND		Ground
A3	+5		Power Supply
A4	A+5		Power Supply for Analog Circuits
A5	-12		Power Supply for RS232C
A6	A1	O	Latched I/O Address Bus
A7	A3	O	↑
A8	A5	O	↑
A9	A7	O	↑
A10	A9	O	↑
A11	A11	O	↑
A12	A13	O	↑
A13	A15	O	↑
A14	ADD17	O	↑
A15	ADD19	O	↑
A16	AEN	O	Address Enable
A17	HRQ	I	Hold Request
A18	DMACLK	O	Clock for DMA Controller (4.77MHz)
A19	WRDMA	O	enable Data Bus to write to I/O when in DMA
A20	COM1	O	Serial I/F Chip Select (RS232C)
A21	XD1	I/O	8 Bits Data Bus for I/O Devices
A22	XD3	I/O	↑
A23	XD5	I/O	↑
A24	XD7	I/O	↑
A25	MEMW	O	Memory Write from CPU
A26	IOW	O	I/O Write from CPU
A27	DRQ0	I	DMA Request Channel 0 (for Memory Refresh)
A28	DRQ2	I	DMA Request Channel 2 (Floppy Disk Control)
A29	DACK0	O	DMA Acknowledge Channel 0 for Memory Refresh
A30	DACK2	O	DMA Acknowledge Channel 2 for FD Control
A31	LCDRDY	O	WAIT to CPU when LCD Controller is active
A32	IRQ6	I	Interrupt Request #6 (for FDC)
A33	NC		No Connection
A34	LED1	O	Floppy Disk Drive A Select

1.5.1 FDC PWB Connector (continued)

Pin number	Signal name	I/O	Remarks
B1	GND		Ground
B2	GND		Ground
B3	+5		Power supply
B4	+12		Power supply for RS232C
B5	A0	O	Latched I/O Address Bus
B6	A2	O	↑
B7	A4	O	↑
B8	A6	O	↑
B9	A8	O	↑
B10	A10	O	↑
B11	A12	O	↑
B12	A14	O	↑
B13	ADD16	O	↑
B14	ADD18	O	↑
B15	UBEN	O	Latched Upper Byte Enable
B16	DMAAEN	O	DMA Address Enable
B17	HOLDA	O	Hold Acknowledge
B18	DMACS	O	DMA Controller Chip Select
B19	FDCS	O	Floppy Disk Controller Chip Select
B20	XD0	I/O	8 Bits Data Bus for I/O Devices
B21	XD2	I/O	↑
B22	XD4	I/O	↑
B23	XD6	I/O	↑
B24	MEMR	O	Memory Read from CPU
B25	IOR	O	I/O Read from CPU
B26	CPURST	O	System Reset
B27	DRQ1	I	DMA Request Channel 1
B28	DRQ3	I	DMA Request Channel 3
B29	DACK1	O	DMA Acknowledge Channel 1
B30	DACK3	O	DMA Acknowledge Channel 3
B31	IRQ4	I	Interrupt Request #4 (RS232C)
B32	NC		No Connection
B33	NC		No Connection
B34	LED2	O	Floppy Disk Drive B Select

1.5.2 Floppy Disk Drive Connector (Same A and B)

Pin number	Signal name	I/O	Remarks
1	NC		No Connection
2	NC		No Connnection
3	GND		Ground
4	NC		No Connection
5	GND		Ground
6	+LED	O	lights on LED when Drive Selected
7	GND		Ground
8	IDX	O	Index(min.1ms Low level Pulse)
9	GND		Ground
10	-DS	O	Drive Select
11	GND		Ground
12	NC		No Connection
13	GND		Ground
14	NC		No Connection
15	GND		Ground
16	-MTR	O	Motor ON
17	GND		Ground
18	DIR	O	Direction of Head Seek
19	GND		Ground
20	STEP	O	Step Pulse(min.1ms Low level pulse)
21	GND		Ground
22	WD	O	Write Date
23	GND		Ground
24	-WREN	O	Write Enable
25	GND		Ground
26	-TKO	O	Track 0
27	GND		Ground
28	-WP	O	Write Protect
29	GND		Ground
30	RDIN	I	Read Date
31	GND		Ground
32	HS	O	Head Select."L"when head1(upper)selected.
33	GND		Ground
34	-RDY	O	Ready

* A is the terminal for drive A and B for drive B.

2. Explanation of IC and I/O

2.1 Processor (CPU)

The MultiSpeed employs a μPD70116D-10 16-bit microprocessor. This processor has a 16-bit data bus and a 20-bit address bus, supporting the 1M-byte address space.

This processor has two built-in 16-bit data buses. This processor operates these two buses in parallel, to reduce the number of processing steps required to execute instructions. This processor, besides, is provided with a built-in EAG (effective address generator), which enables high-speed calculation of effective addresses in all addressing modes, which is required for memory accessing. This processor, moreover, has a 16/32-bit temporary register/shifter (hardware) to process multiplication, division, and shift/rotation instructions for the purpose of higher processing.

The user can select as this processor clock frequency 4.77 MHz or 9.54 MHz.

* Programming considerations

This processor uses four 16-bit general registers, AX, BX, CX, and DX. Each can be used as a 16-bit register and can also be divided into two 8-bit registers of high-order and low-order (AH, AL, BH, BL, CH, CL, DH, and DL).

Those general registers can also be used as the default register to process special instructions as shown in Fig. 2.1.1 below.

Fig. 2.1.1 Default registers

AX	Word multiplication/division, word input/output, interpretation, BCD (binary coded decimal) rotation, data conversion
AL	Byte multiplication/division, byte input/output, BCD rotation, byte conversion
AH	Byte multiplication/division
BX	Interpretation
CX	Loop control branch, repeat prefix
CL	Shift instruction, rotation instruction, BCD operation
DX	Word multiplication/division, indirect addressing input/output

Besides those general registers, this processor has a 16-bit register called program status word. This register consists of two flags: control flag which controls processor operation and status flag which automatically changes based on the result of instruction execution so as to indicate the system status.

The control flag comes in four types: MD (mode), DIR (direction), IE (interrupt enable), and BRK (break);

while the status flag comes in six types: V (overflow), S (sign), Z (zero), AC (auxiliary carry), P (parity), and CY (carry). Out of these, the CY flag can directly be set, reset, and reversed by instructions. These flags are arrayed on the program status word in the configuration shown in Fig. 2.1.2.

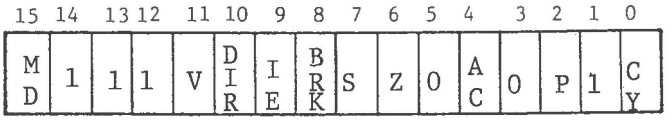


Fig. 2.1.2 Program status word

2.2 Clock Pulse Generator

This clock pulse generator is built in the IC SLA6170FIK gate array to generate the clock pulse used by the processor or other devices. This clock pulse may come in a frequency of 4.77 MHz or 9.54 MHz, which can be switched by turning bit 4 of the dip switch on the rear panel of the MultiSpeed body on and off respectively. Moreover, when bit 4 of the dip switch is set to off to provide a frequency of 9.54 MHz, the clock frequency can be switched by software.

This clock pulse generator divides the source frequency of 19.090906 MHz by four into 4.77 MHz and by two into 9.54 MHz. Both frequencies have the same duty ratio of 50%.

* Programming considerations

To switch the clock frequency by software, the above-mentioned dip switch (bit 4) must be set to OFF (9.54 MHz) beforehand. Then, the operator can switch the frequency by setting or resetting the MSB (D7) of the clock/character generator (CG)/ROM mapping register in I/O address E0 (hex). By setting the MSB to 0, the clock frequency is switched to 4.77 MHz, and by setting it to 1, 9.54 MHz.

The other bits of this register are detailed later.

2.3 System Timer

As the system timer this processor employs a μPD71054 programmable timer counter. This timer has three counters which operate mutually independently: counter #0 as software interrupt counter, counter #1 to control the refresh timing for the direct memory access controller, and counter #2 to support the tone generator for the speaker.

These three built-in counters use the same clock frequency obtained by dividing a frequency of 4.77 MHz by two. With this, those counters have the same minimum timing resolution of 420 nsec.

* Programming considerations

This system timer can be programmed by writing both the control word which specifies the operation mode of each built-in counter and the upper limit count value. With this, those built-in counters operate as a count-down counter.

Before use, first specify the desired operation mode of each counter with the control word. A mode once programmed into the counter remains unchanged until it is switched to a different one.

Next, write a count value to the count register for each counter. Immediately after the count value thus written is transferred from the count register to the down counter, it starts counting.

The control word must be written to I/O address 043 (hex) and the count value, to 040(hex) through 042(hex).

The operator can read out the current count data during counting. To do so, he must use the count latch command or multiple latch command. With this, he can read it out without affecting timer operation.

Some bits of the 061(hex) port B or 062(hex) port C are used to stop, start, and detect the output of the counting by counter #2 (for tone generator).

Fig. 2.3.1 Timer control register

Address (hex)	R/W	Usage
040	R/W	Counter #0
041	R/W	Counter #1
042	R/W	Counter #2
043	W	Timer control word register
061	W	Port B
062	R	Port C

Timer Control Word Register: 043(hex)

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	RWM1	RWM0	CM2	CM1	CM0	BCD

Bit Usage

7 - 6 Counter selection or multiple latch command

SC1	SC0	
0	0	: Counter #0
0	1	: Counter #1
1	0	: Counter #2
1	1	: Multiple latch command

5 - 4 Read/Write mode

RWM1	RWM0	
0	0	: Count latch command
0	1	: Low-order byte read/write
1	0	: High-order byte read/write
1	1	: Read/write of low-order and high-order bytes in this order

3 - 1 Count mode

CM2	CM1	CM0	
0	0	0	: Mode 0
0	0	1	: Mode 1
-	1	0	: Mode 2
-	1	1	: Mode 3
1	0	0	: Mode 4
1	0	1	: Mode 5

0 Binary or BCD counting

0 : Binary counting (16 digits)
1 : BCD counting (4 digits)

Port B : 061(hex)

Some bits of the port B register are used for the system timer. The other bits are explained as required.

Bit	Usage
0	Enables output of the counter #2 content. Counter #2 is stopped by setting this bit to 0.

Port C : 062 (hex)

Some bits of the Port C register are used for the system timer. The other bits are explained as required.

Bit	Usage
5	Counter #2 output. When this bit is detected, the application program can monitor the output of counter #2.

2.4 Interrupt Controller

As the interrupt controller the MultiSpeed employs the μPD71059G interrupt control unit.

This programmable interrupt controller enables the operator to change the priority of interrupt requests, mask interrupts at a desired interrupt level, and set the interrupt routine address, etc. by transferring the command word from the processor. This interrupt controller is used in the edge trigger mode by the MultiSpeed.

The MultiSpeed hardware interrupt comes in eight levels of maskable interrupts (levels 0 to 7) and one nonmaskable interrupt (NMI) that cannot be masked by software. As for the priority order of those interrupt levels, the NMI has always the highest one, followed by levels 0 to 7 which can be programmed. Upon power application, the NMI is automatically given the highest priority, followed by levels 0 to 7 in this order as a result of initialization.

Levels 0 through 7, which are programmable, are of the rotating priority system, so that once the lowest level is specified, the other levels are automatically determined. Note here that interrupt levels 0 to 7 are assigned to processor interrupt vectors 8 to 15 respectively. Fig. 2.4.1 below gives the hardware interrupt levels.

Fig. 2.4.1 Hardware interrupt levels

Interrupt	Usage
NMI	Power fail/Power switch
0	Timer
1	Keyboard
2	Reserved
3	Asynchronous Communications (RS-232C)
4	Asynchronous Communications (Modem)
5	Reserved
6	Diskette
7	Printer

* Programming considerations

The control words used by this interrupt controller can roughly be divided into two groups: initialize word and command word.

The initialize word comes in four types, IW1 to IW4, for initialization of the interrupt controller, which requires for starting general processing that proper information should be written to those four words. In the MultiSpeed, however, IW3 is not used because the interrupt controller is not connected in a cascade.

The command word, on the other hand, comes in three types: the interrupt mask word (IMW), priority and

finish control word (PFCW), and mode control word (MCW). Those three words are used to give the necessary commands to the interrupt controller for the purpose of masking interrupt requests, changing the priority, and terminating interrupt processing.

This interrupt controller enters the initialize sequence immediately after IW1 is written to I/O address 020 (hex). Immediately after IW2 and IW4 are both written to address 021 (hex), the initialization of the interrupt controller is completed.

Once the interrupt controller completely passes the initialize sequence, the operator can give command words as he likes. The IMW and the PFCW and MCW are set to addresses 021 (hex) and 020 (hex) respectively. Into address 020 (hex) appears the information of the built-in register of interrupt controller read out with the MCW. The NMI for the MultiSpeed uses some bits of address 0A0 (hex). Fig. 2.4.2 lists the interrupt and NMI control registers.

Fig. 2.4.2 Interrupt and NMI control registers

Address (hex)	R/W	Usage
020	W	Initial word 1 (IW1)
	W	Priority and finish control word (PFCW)
	W	Mode control word (MCW)
	R	Interrupt request register
	R	Interrupt in-service register
	R	Polling data
021	W	Initial word 2 (IW2)
	W	Initial word 4 (IW4)
	R/W	Interrupt mask word (IMW)
0A*	W	NMI Mask Register

Note: The address marked * is a "don't-care" one.

NMI Mask Register (0A* (hex))

The NMI (nonmaskable interrupt) occurs if the power switch is turned off or if the power voltage drops below 9.3 V. Such NMIs can be masked using some bits of the NMI mask register, as follows:

Bit	Usage
7	'0': Disable NMI
	'1': Enable NMI

Command Word Formats

·Interrupt Mask Word (IMW)

This word masks the interrupt request register (IRR) so as to inhibit interrupt requesting at the relevant interrupt level. This word also masks the interrupt in-service register (ISR) in the exception nest mode.

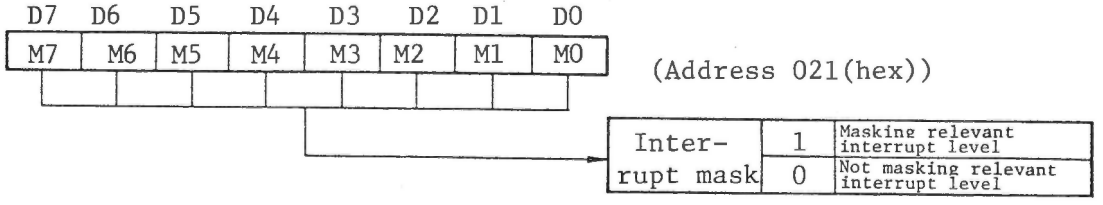


Fig. 2.4.3 Interrupt mask word

·Priority and Finish Control Word (PFCW)

This word is used to set the command which notifies the interrupt controller of the termination of interrupt processing or change (rotate) the interrupt request priority.

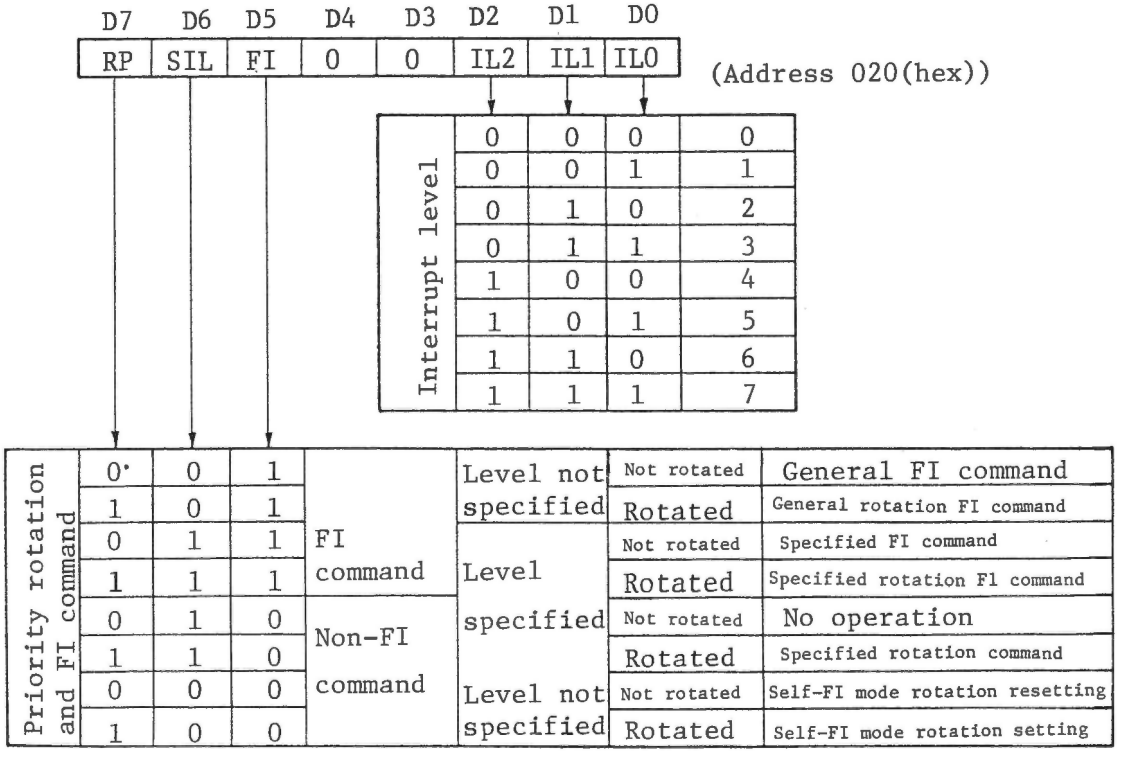


Fig. 2.4.4 Priority and Finish Control Word

·Mode Control Word (MCW)

This word is used to make polling, set read-out registers, or set the exception nest mode.

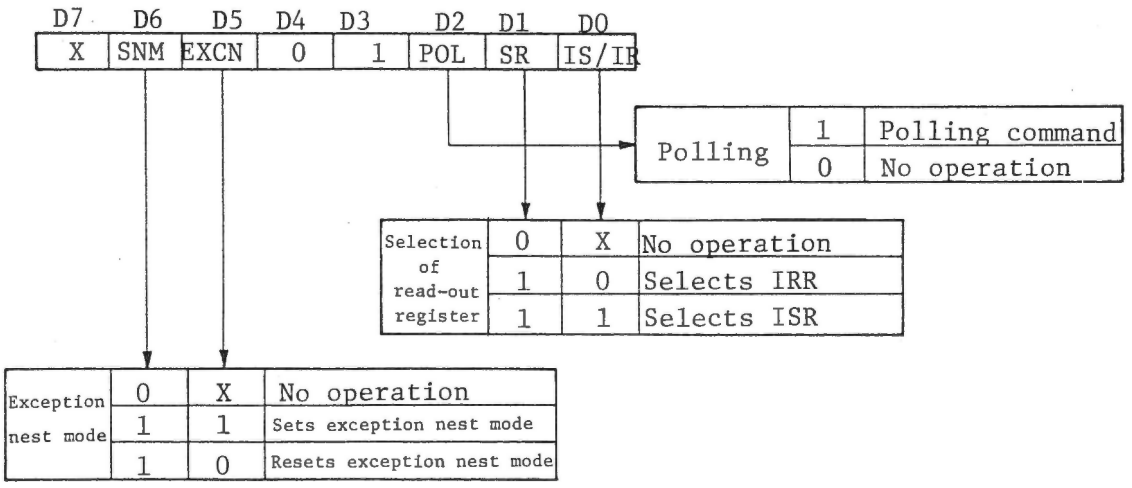


Fig. 2.4.5 Mode control word

2.5 Direct Memory Access (DMA) Controller

As the direct memory access (DMA) controller the Multi-Speed employs the 82C37-5 programmable DMA controller. This DMA controller enables high-speed data transfer because there need not be intervention by the processor over the peripherals mounted for data transfer among memory I/O devices and, moreover, it will not take in data which it transfers itself.

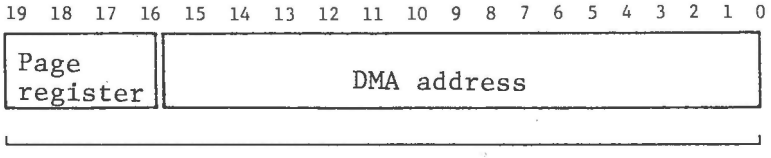
This DMA controller has four programmable DMA channels (channel numbers 0 to 3), each of which can be controlled independently. This DMA controller comes in three transfer modes, the single, block, and demand transfer modes, so that the operator can select and set, for each channel, auto initialize inhibition, DMA transfer inhibition, transfer address incrementing, or transfer address decrementing. Channel #0, however, is exclusively used for memory refreshing and channel #2, for DMA transfer between the floppy disk and memory.

Data transfer in the single mode requires for operation six clock pulses (1.25 ms) for each byte. Both the block mode and the demand mode require that at least three clocks (0.63 ms) each should be given for the second byte and subsequent bytes. This DMA controller uses a clock frequency of 4.77 MHz.

The priority for these channels is fixed in such a way that channel #0 has the highest priority, followed by channel #1 to channel #3 in this order. This system, however, does not support either inter-memory data transfer or cascading.

* Programming considerations

This DMA controller has a built-in address register of 16-bit configuration, so that it supports 20-bit addresses by providing a 4-bit page register for each DMA channel in addresses 080 (hex) through 083 (hex). Each page register is allocated to the high-order four bits of the 20-bit DMA transfer address as shown in Fig. 3.5.1. The page register for channel #0, however, cannot be used.



DMA address bit configuration

Fig. 3.5.1 DMA address configuration

This DMA controller uses such registers as listed in Fig. 3.5.2, to set the DMA operation mode or transfer address and the transfer data count value or each read out channel status by use of the processor.

Fig. 3.5.2 DMA controller registers

Address (hex)	R/W	Usage
000	R/W	Channel #0 current address register
001	R/W	Channel #0 current word count register
002	R/W	Channel #1 current address register
003	R/W	Channel #1 current word count register
004	R/W	Channel #2 current address register
005	R/W	Channel #2 current word count register
006	R/W	Channel #3 current address register
007	R/W	Channel #3 current word count register
008	R	Status register
	W	Command register
009		Request register
00A		Single mask register
00B		Mode register
00C	W	Clear first last F/F
00D	W	Mask clear register
00E	W	Clear-mask register
00F	W	All-mask register
080		Not used
081	W	Channel #2 page register
082	W	Channel #3 page register
083	W	Channel #1 page register

DMA Command Register: 008 (hex)

Only some bits of the DMA command register can be set by the user, the other bits being automatically initialized upon system start-up.

Bit	Usage
2	Disables the DMA controller. If this bit is set to 1, data transfer is inhibited over all DMA channels.

DMA Status Register: 008 (hex)

Bit	Usage
7	Channel #3 request 0: Not requested 1: Requested
6	Channel #2 request 0: Not requested 1: Requested
5	Channel #1 request 0: Not requested 1: Requested
4	Channel #0 request 0: Not requested 1: Requested
3	Channel #3 terminal count 0: Terminal count is not reached. 1: Terminal count is reached.
2	Channel #2 terminal count 0: Terminal count is not reached. 1: Terminal count is reached.

1	Channel #1 terminal count
	0: Terminal count is not reached.
	1: Terminal count is reached.
0	Channel #0 terminal count
	0: Terminal count is not reached.
	1: Terminal count is reached.

Request Register: 009 (hex)

The request register is used to make software requests like DMA requests from peripherals.

Bit	
7 - 3	Not used
2	Request bit
	0: The request is reset.
	1: The request is set.
1 - 0	Channel specification bit
	00: Channel #0
	01: Channel #1
	10: Channel #2
	11: Channel #3

Single Mask Register: 00A (hex)

Bit	Usage
7 - 3	Not used
2	Mask bit
	0: Masking is reset.
	1: Masking is set.

1 - 0	Channel specification
	00: Not used
	01: Channel #1
	10: Channel #2
	11: Channel #3

Mode Register

The mode register is used to set the operation mode for each channel.

Bit	Usage
7 - 6	Transfer mode specification
	00: Demand transfer mode
	01: Single transfer mode
	10: Block transfer mode
	11: Cascade mode
5	Address incrementing/decrementing
	0: Address incrementing
	1: Address decrementing
4	Auto initialization permitted/not permitted
	0: Auto initialization not permitted
	1: Auto initialization permitted
3 - 2	Transfer direction setting (transfer request)
	00: Verify transfer
	01: Write transfer
	10: Read transfer
	11: Transfer inhibited

1 - 0 Channel specification

00: Channel #0

01: Channel #1

10: Channel #2

11: Channel #3

Clear First/Last F/F: 00C (hex)

This F/F (flip-flop) acts as a software command.

The DMA controller of the MultiSpeed transfers the content of the 16-bit address or word count register twice for the high-order eight bits and the low-order eight bits each. For this purpose, the first/last F/F is used to judge the high-order bits and the low-order bits in such a way that when this F/F is reset the low-order bits are transferred and when it is set the high-order bits are transferred. By resetting this F/F, the low-order eight bits can be accessed.

Master Clear Register: 00D (hex)

This register acts as a software command, to set the mask register and reset the contents of the command, status (low-order four bits), request, and temporary registers as well as of the first/last F/F. This master clear command,

when executed, permits the DMA controller to enter the idle cycle.

Clear Mask Register: 00E (hex)

This register acts as a software command. This command, when executed, resets the mask bit of all DMA channels, so that DMA transfer is accepted.

All Mask Register: 00F (hex)

This register gives a direction to permit or inhibit data transfer for all channels at a time.

Bit	Usage
7 - 4	Not used
3	Channel #3 mask
	0: Reset
	1: Set
2	Channel #2 mask
	0: Reset
	1: Set
1	Channel #1 mask
	0: Reset
	1: Set
0	Not used

2.6 Random Access Memory (RAM) Region

This RAM region comprises the 512K-byte non-backup RAM, 128K-byte backup RAM, and 16K-byte video RAM. Addresses 80,000 (hex) and subsequent are covered by the static RAM, while addresses 00,000 (hex) through 7F,FFF (hex) are covered by the pseudo-static RAM, which needs refreshing. This RAM area of the MultiSpeed does not have a parity bit.

The RAM address starts with 00,000 (hex), whose subsequent addresses are assigned as shown in Fig. 3.6.1.

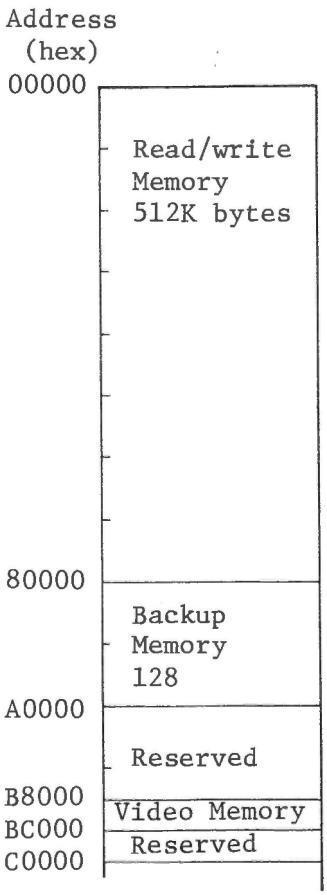


Fig. 3.6.1 RAM map

* Programming considerations

As many as 128K bytes of addresses starting from RAM address 80,000 (hex) are allocated in the backup RAM area, which can be used only by the system. In order to not destroy the data stored in this system area, the user should not use that area.

2.7 Read Only Memory (ROM) Region

This ROM region comprises a 512K-byte area, to cover addresses C0,000 (hex) through FF,FFF (hex).

A ROM region area of addresses D0,000 (hex) through EF,FFF (hex), which has a capacity of 128K bytes, can be switched in three ways as a bank so as to be used as an area having a capacity of 384K bytes. By adding expansion ROM devices, this area can be extended to five banks (640K bytes), so that the ROM region can be expanded to 768K bytes as a whole.

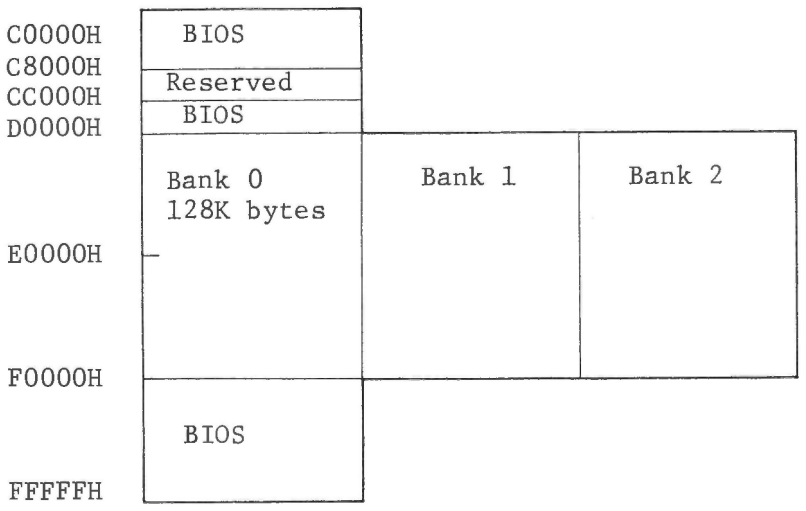


Fig. 2.7.1 ROM map

* Programming considerations

To access the intra-ROM region bank, the currently used bank must be switched to that bank desired. For bank switch-over, the CLK/CG/ROM mapping register in address 0E0 (hex) is used.

CLK/CG/ROM Mapping Register: 0E0 (hex)

Some bits of this register are used to specify a desired ROM bank (bank switch-over). The other bits are explained as required.

Bit	Usage
2 - 0	ROM bank #
	000: Bank #0
	001: Bank #1
	010: Bank #2
	011: Bank #3 (Expansion ROM)
	100: Bank #4 (Expansion ROM)

2.8 Floppy Disk Drives (FDDs)

The MultiSpeed employs a disk unit which comprises two floppy disk drives (FDDs) for handling 3.5-inch micro-floppy disks. Both of these drives are compatible with IBM-formatted floppy disks, supporting double-sided double-density floppy disks to provide a capacity of 720K bytes per drive after being formatted.

When a floppy disk is inserted into the slot of this floppy disk drive and set to it, the floppy disk is first chucked internally by the spindle motor, which automatically rotates. This automatic chucking takes 800 ms at most.

After the floppy disk is correctly set to the read/write drive, the spindle motor starts rotating to rotate the floppy disk. The disk rotating speed is stabilized by the frequency servo to a constant value of 300 revolutions per minute (RPM).

The track movement mechanism which moves the magnetic head is driven by a stepping motor. The stepping motor moves the magnetic head by one track of distance per stepping pulse. It takes 6 ms.

Data can be recorded to floppy disks by using the modified frequency modulation (MFM) system, so that the floppy

disk controller can decode data to be recorded and encode the data read out. The effective track width, after recording, is 0.115 mm and the track pitch is 0.1875 mm, so that the track density is 135 tracks per inch (tpi). The magnetic head can seek desired data irrespective of whether the spindle motor is rotating or not, so that the system can activate the spindle motor and also seek desired data at the same time.

Each floppy disk drive has the following built-in sensors, whose output is sent to and used by the floppy disk controller, which in turn controls the operation of the drive.

- Sensor which detects whether the head is positioned to track 00 (the outermost track)
- Sensor which detects the start point of a track (This sensor actually detects the index hole.)
- Sensor which detects whether the write inhibit hole is made (write-protected) or not
- Sensor whether a floppy disk is taken out of the drive

2.9 Floppy Disk Controller (FDC)

The MultiSpeed employs as the floppy disk controller (FDC) the μPD-72065G programmable floppy disk controller. This controller is positioned between the system bus and the floppy disk drive (FDD) to control the FDD operation and relay the data transferred between the FDD and the system data bus.

Data (8-bit parallel data) are transferred from memory via the data bus to the FDC, which in turn converts those data to serial data and then sends them to the FDD with both a timing clock and a cyclic redundancy code (CRC) attached to them. At the FDC the serial data read out from the FDD undergo such processes as CRC checking, separation of clock and data, and conversion into parallel data, which are then transferred to memory via the system data bus.

The direct memory access (DMA) method is employed in data transfer between memory and the FDC. The FDC, moreover, causes a hardware interrupt of level 6 either when a read/write operation to a floppy disk is terminated or when a request must be made to the processor to read the status of the FDC itself.

The FDC supports the recording system of such sepcifications as double-sided, double-density, and modified frequency modulation (MFM), providing the floppy disk format compatibilities with the IBM.

The FDC is provided with a standby function to reduce power consumption. With the standby function, the FDC is automatically powered off when it is not accessed by the system. In the standby mode, therefore, disk accessing takes a long time as compared with that in the general mode. The FDC can be set in the standby mode by MultiSpeed application " Setup " as well as by the BIOS routine.

By connecting the external floppy disk controller (EXT. FDC) connector on the MultiSpeed body rear pannel to the IBM personal computer at its expansion drive connector, the 3.5-inch MultiSpeed FDD can be used as an expansion drive of that IBM machine. In this case, the FDC of Multi-Speed itself is disconnected from the system.

* Programming considerations

The FDC uses the following registers, listed below, to provide control by software or read out the FDC status or data.

(hex)	R/W	Usage
3F2	W	FDC Control Register
3F4	R	FDC Status Register
3F5	R/W	FDC Data Register

FDC Control Register: 3F2 (hex)

The FDC control register (DOR) is used, for example, to select drives, turn the drive spindle motor ON/OFF, reset

the FDC, or enable DMA or interrupts.

Bit	Usage
7 - 6	Not used
5	Drive B motor on
4	Drive A Motor on
3	Enable FDC Interrupt/DMA

This bit enables both FDC interrupt requests and DMA transfer requests. If this bit is reset, neither the FDC interrupt request nor the DMA transfer request is enabled.

2	FDC Reset

This bit, when set to 0, resets the FDC and fixes it in idle status. This bit is set by the program which enables the FDC.

1 - 0	Drive Select

These bits are decoded to select the desired drive. These bits, however, are ignored if the drive thus selected has already been set off by bit 4 or 5.

Bit	
10	Drive
00	Drive A
01	Drive B
10	Not used
11	Not used

FDC Status Register: 3F4 (hex)

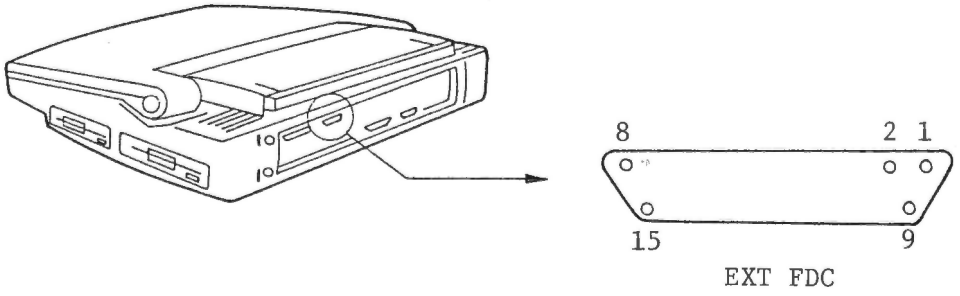
Bit	Usage
7	Request for master. Indicates whether the FDC data register is ready for read/write operation. When this bit is 1, the data register is ready.
6	Data Input/Output Indicates the direction in which data are transferred between the processor and the FDC data register, as follows: 0: Data are transferred from the processor to the data register. 1: Data are transferred from the data register to the processor.
5	Non-DMA mode When this bit is 1, the FDC operates in non-DMA mode. (The DMA system is not used in data transfer.)
4	FDC Busy Indicates that the FDC is in read, write, or seek operation.
3 - 2	Reserved
1	FDD-B Busy Indicates that drive B is in the seek mode.
0	FDD-A Busy Indicates that drive A is in the seek mode.

FDC Data Register: 3F5 (hex)

This 8-bit register actually comprises multiple sub-registers, each of which can be read out for each access. These sub-registers store the data, command, parameter, and FDD status information. Data bytes read out of or written to this register are used to obtain the results of executing programs or special commands.

2.10 External Floppy Disk Controller (EXT FDC) Interface

This interface, a 15-pin connector, is used to connect the FDD built in the MultiSpeed to the IBM personal computer's floppy disk controller. To actually connect them, the "IBM cable kit" is employed. What follows will explain the pins of this connector. In the following explanation, the plus (+) or minus (-) sign immediately preceding the signal name indicates the active state of the relevant signal. Also, I (input) or O (output) given in the I/O column in the table below indicates the signal feeding direction as viewed from the connector.



EXT FDC

Pin No.	Signal name	I/O	Explanation
1	- Index	O	This negative-logic pulse signal indicates the start point for tracks; as many a one is given for each revolution of the disk.
2	- Motor 3 Enable	I	This signal, when set to the low level, turns on the motor for MultiSpeed drive A.
3	- Drive 4 Select	I	This signal selects MultiSpeed drive B.
4	- Drive 3 Select	I	This signal selects MultiSpeed drive A.
5	- Motor 4 Enable	I	This signal, when set to the low level, turns the motor on for MultiSpeed drive B.
6	- Direction	I	This signal specifies the direction in which to move the read/write head, when the step signal is received. This signal moves the head to the center of the disk when it is set to low level. When it is sent to high level, it moves the head to the outermost track of the disk.
7	- Step	I	This signal moves the read/write head by as much as one track per pulse.

Pin No.	Signal name	I/O	Explanation
8	- Write Data	I	This signal, when the Write Enable signal is active, is recorded as a change in magnetism, onto disks.
9	- Write Enable	I	This signal, when set to low level, enables data to be written to disks.
10	- Track 0	O	This signal, when set to low level, indicates that the head for a selected drive is positioned at the outermost track.
11	- Write Protect	O	This signal, when set to low level, indicates that a selected drive is write-protected.
12	- Read Data	O	This is the regenerative pulse signal which indicates the information recorded on disks.
13	- Head Select	I	This signal, when set to low level, selects the upper head of a selected drive.
14	GND		
15	GND		

2.11 Real-Time Clock

As the real-time clock the MultiSpeed employs the RTC-58321. The real-time clock has its own built-in crystal oscillator, to support the timer function and the 100-year calendar.

The timer function enables the user to select the 12-hour mode or the 24-hour mode, supplying the count data for time (hour, minute, and second). The calendar, on the other hand, supports a function to automatically adjust month-end dates and leap years.

* Programming considerations

One or two counters are provided to correspond to each of the year, month, day, day-of-the-week, hour, minute, and second data. Each of those counters is assigned a 4-bit internal address, to count 4-bit data. The count data can be read or written by writing the corresponding internal address content to I/O address 0E4(hex) and subsequently specifying read or write operation respectively; one counter of data is read or written each time this operation is executed. However, the internal address cords, hex D, hex E and hex F, are not used to specify any internal counter. Those internal address cords are interpreted as the command for the real-time clock.

Fig. 2.11.1 gives the correspondence between the internal counter and the internal address.

Fig. 2.11.1 Internal counters and internal address

Internal address (hex)	Internal counter	Count value	Usage	
0	S1	0 – 9	Low-order digit	Second
1	S2	0 - 5	High-order digit	
2	M11	0 - 9	Low-order digit	Minute
3	M12	0 - 5	High-order digit	
4	H1	0 – 9	Low-order digit	Hour
5	H2	0-1/0-2	High-order digit	
6	W	0 – 6	Day-of-the-week	
7	D1	0 – 9	Low-order digit	Day
8	D2	0 – 3	High-order digit	
9	M01	0 – 9	Low-order digit	Month
A	M02	0 - 1	High-order digit	
B	Y1	0 – 9	Low-order digit	Year
C	Y2	0 – 9	High-order digit	
D	-		Counter resetting	
E - F	-		Reference signal output	

Real-Time Clock Control Register (Calendar Chip): 0E4(hex)

This register is used to read the time or date data from or write it to the real-time clock, specifically storing the counter's internal address, read/write direction, etc.

When the register is written;

7	6	5	4	3	2	1	0
CS	DIR	AWS	RD/WR	D3	D2	D1	D0

Bit	Usage
7	Chip Select bit. This bit is set to 1 in all cases in which data is written.
6	Direction bit 1: Data/internal address contents are written in. 0: Data is read out.
5	Address Write Strobe bit. When this bit is set to 1, the content of the four low-order bits of this register is latched as the internal address.
4	Read/Write Strobe bit. When this bit is set to 1, the system executes read/write operation to the counter of an internal address which has been latched, with the low-order four bits of this register assumed to be the count data.

3 - 0 These four bits store the internal address of count data to be written in. The LSB is bit 0.

When the register is read:

7	6	5	4	3	2	1	0
BUSY	—	—	—	D3	D2	D1	D0

Bit	Usage
7	Real-time clock busy bit
6 - 4	Not used
3 - 0	These four bits store count data read out. The LSB is bit 0.

Fig. 2.11.2 below shows a timing chart for internal counter read/write operation by combination of the high-order four bits.

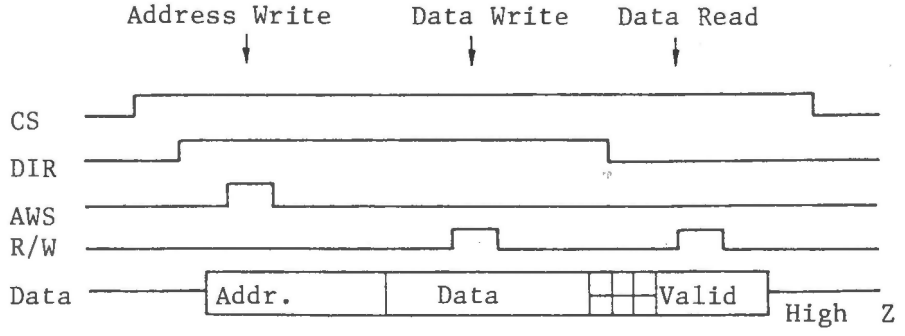


Fig. 2.11.2 Timing chart for count data read/write operation

H2 Counter: Internal address 5(hex)

This counter counts the high-order digit ("10s" digit) of the hour data.

Bit	Usage
3	This bit selects the 24-hour/12-hour mode. If this bit is set to 1, bit 2 is automatically reset to 0. 0: 12-hour mode 1: 24-hour mode
2	0 = AM 1 = PM
1 - 0	These two bits are used to count the high-order digit of the hour data.

D2 Counter: Internal address 8(hex)

This counter counts the high-order digit ("10s" digit) of the date.

Bit	Usage
3 - 2	These bits are used to select the leap year mode as follows: 00: The leap year mode is entered if the remainder is 0 as a result of dividing the year according to the Julian calendar by 4. 01: The leap year mode is entered if the remainder is 3 as a result of dividing the year value by 4.

10: The leap year mode is entered if the remainder is 2 as a result of dividing the year value by 4.

11: The leap year mode is entered if the remainder is 1 as a result of dividing the year value by 4.

1 - 0 These bits are used to count the high-order digit of the date data.

Reretting counter: Internal address D(hex)

The D(hex) internal address content can be written as the command to I/O address 0E4(hex) to be latched into the real-time clock, then read out to reset all internal counters for this clock to 0. Note here that the real time clock cannot be reset by pressing the reset switch mounted on the rear panel of the MultiSpeed.

Reference signal output: Internal address E(hex) and F(hex)

The E(hex) or F(hex) internal address content can be written to I/O address 0E4(hex) to be latched into the real-time clock then read out, to feed the reference signal to the low-order four bits of the I/O address 0E4(hex).

Bit	Output frequency (Hz)	Pulse width (μs)	Output logic (positive/negative logic)
3	1/3600	122.1	Negative logic
2	1/60	122.1	Negative logic
1	1	122.1	Negative logic
0	1024	488.3	Positive logic

2.12 Outline of Gate Arrays

The SLA6170xxx is a gate array device for 80-pin/1700-gate, having the following functions.

SLA6170F1K (CTL)

1. Bus controller (μPD71088 equivalent)
2. Clock generator (μPD71011 equivalent)
3. I/O Chip Select decoder
4. Reset circuit
5. Interrupt/NMI processor
6. Weight
7. External ROM Chip Select decoder
8. E0 port

SLA6170F1M (MM)

1. Main memory Chip Select decoder
2. Refresh circuit
3. Highest-order address latch
4. BIOS/AP ROM Chip Select decoder

SLA6170F1J (LD)

1. Peripheral circuit for LCD/CRT controller
2. I/O data bus 16-bit/8-bit switch-over unit

SLA6170F1L (IOP)

1. Printer/keyboard port (μPD71055 equivalent)
2. E4 port/E8 port
3. Audio control

The μPD65013G-096 is a gate array device for 100-pin/1300-gate, having the following functions:

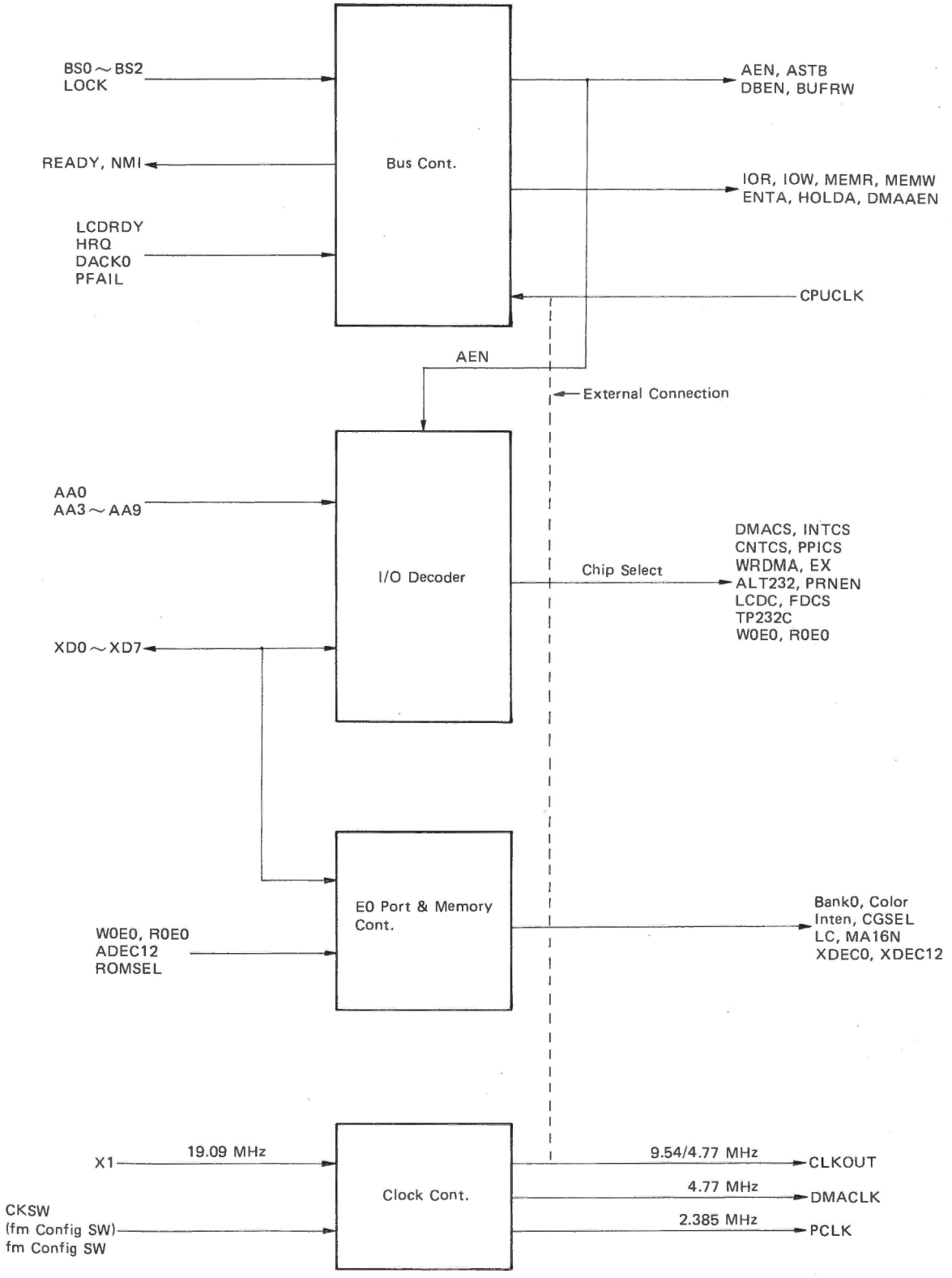
- o Peripheral circuit for DMAC
- o Peripheral circuit for FDC
- o Other miscellaneous circuits

2.12.1 SLA6170F1K (Gate Array #1) Pin Assignment

Pin number	Signal name	I/O	Remarks
1	MA16	I	address bit 16 for memory
2	LBANK0	O	external ROM BANK select(even address)
3	HRA16	O	external ROM BANK select(odd address)
4	EXRCS1	O	external ROM chip select #1
5	EXRCS2	O	external ROM chip select #2
6	EXRCS3	O	no use
7	EXRCS4	O	no use
8	W0E0	I	write enable to port E0h
9	R0E0	I	read enable from port E0h
10	CKSW	I	position of CONFIG SW 4. 9.5MHz when "H"
11	DMACLK	O	clock for DMA controller (4.77MHz)
12	Vss(GND)	P	ground
13	X1	I	input from clock osciator (19.09MHz)
14	CLKOUT	O	system clock (9.54/4.77MHz)
15	PCLK	O	2.38MHz
16	READY	O	CPU ready
17	RESET	O	no use
18	BUFRW	O	controls direction of data bus buffer
19	DBEN	O	open the data bus buffer
20	INTA	O	inerrupt acknowledge
21	ASTB	O	address strobe
22	BS0	I	bus status from CPU #0
23	BS1	I	bus status from CPU #1
24	BS2	I	bus status from CPU #2
25	IOR	I/O	I/O read
26	MEMR	I/O	memory read
27	IOW	I/O	I/O write
28	MEMW	I/O	memory write
29	AEN	O	address enable from CPU
30	LCDRDY	I	WAIT from LCD controller to CPU
31	DWAIT	O	no use
32	LOCK	I	BUSLOCK from CPU
33	HRQ	I	Hold Request to CPU when in DMA
34	DMAAEN	O	address enable when in DMA
35	HOLDA	O	Hold acknowledge from CPU when in DMA
36	PFAIL	I	"H" when power fail occured
37	NM1	O	Non Mascable Interrupt to CPU
38	MRES	I	Master reset
39	DACK0	I	DMA acknowledge #0 for memory refresh
40	ADEC12	I	decoded upper memory address

Pin number	Signal name	I/O	Remarks
41	XDEC0	O	ROM BANK #0 select
42	XDEC12	O	ROM BANK #1,#2 select
43	CPUCLK	I	connect No.14pin
44	MA16N	O	inverted memory address 16
45	XD7	I/O	8bits data bus for I/O devices
46	XD6	I/O	↑
47	XD5	I/O	↑
48	XD4	I/O	↑
49	XD3	I/O	↑
50	XD2	I/O	↑
51	XD1	I/O	↑
52	XD0	I/O	↑
53	Vdd(+5V)	P	power supply
54	BANK0	O	inverted ROM BANK SELECT BIT 0 at E0h
55	COLOR	O	"H" when LCDC is in color mode
56	INTEN	O	"H" when intensity bit is enable
57	CGSEL	O	select font in CG ROM
58	LC	O	"L" when screen device is LCD
59	TEST1	I	TEST pin (connect to ground)
60	ROMSEL	I	position of CONFIG SW 3. "L" when 1M ROM
61	UBE	I	Latched UPPER BYTE ENABLE
62	AA9	I	address bus for I/O devices
63	AA8	I	↑
64	AA7	I	↑
65	AA6	I	↑
66	AA5	I	↑
67	AA4	I	↑
68	AA3	I	↑
69	AA0	I	↑
70	DMACS	O	DMA controller chip select
71	INTCS	O	interrupt controller chip celect
72	CNTCS	O	counter chip select
73	PPICS	O	parallel I/F chip select
74	WRDMA	O	enable data bus to write to I/O when in DMA
75	EX	O	enables port E0h,E4h,E8h
76	ALT232	O	MODEM chip select
77	PRNEN	O	printer enable
78	LCDC	O	LCD controller chip select
79	FDCS	O	Floppy Disk Controller chip select
80	TP232	O	Serial I/F chip select (to 82C50)

SLA6170 F1K (Gate Array #1) Function Diagram

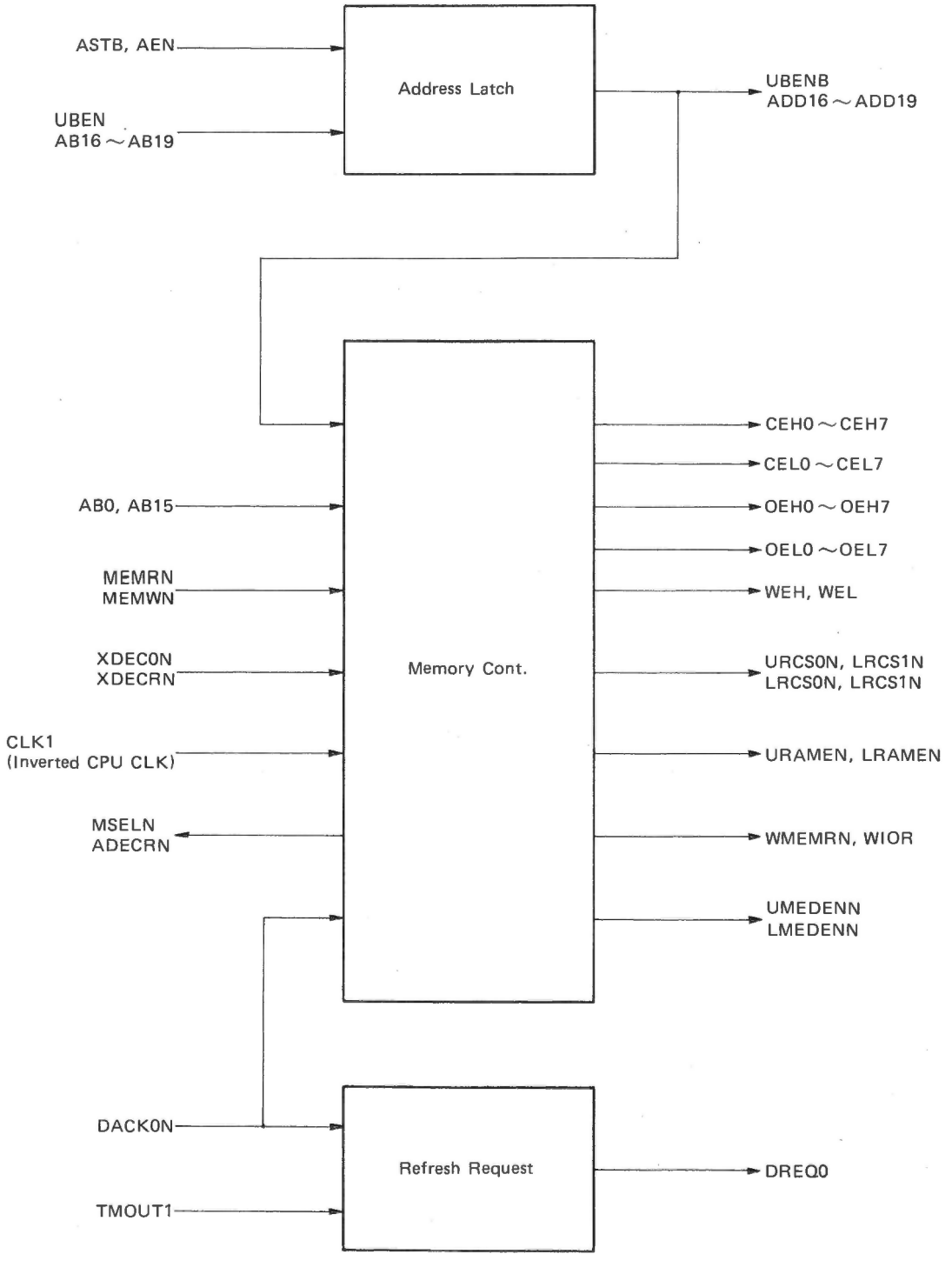


2.12.2 SLA6170F1M (Gate Array #2) Pin Assignment

Pin number	Signal name	I/O	Remarks
1	UBEN	I	Upper Byte Enable from CPU
2	AB19	I	Upper address bus from CPU
3	AB18	I	↑
4	AB17	I	↑
5	AB16	I	↑
6	AEN	I	address enable
7	ASTB	I	address strobe
8	IORN	I	I/O read
9	WIOR	O	wide I/O read
10	Vdd(+5V)	P	power supply
11	CLK1	I	inverted system clock
12	Vss(GND)	P	ground
13	URAMEN	O	RAM enable (odd address)
14	LRAMEN	O	RAM enable (even address)
15	MSELN	O	decoded upper address bit
16	Vss(GND)	P	ground
17	TMOUT1	I	output from counter for memory refresh
18	DREQ0	O	DMA request channel 0 for memory refresh
19	UMDENN	O	memory data enable (odd address)
20	LMDENN	O	memory data enable (even address)
21	EXTONN	I	no use
22	* *		no use
23	* *		no use
24	MEMRN	I	memory read
25	MEMWN	I	mamory write
26	DACK0N	I	DMA acknowledge channel 0 for memory refresh
27	URCS0N	O	ROM chip select 0 (odd address)
28	LRCS0N	O	ROM chip select 0 (even address)
29	URCS1N	O	ROM chip select 1 (odd address)
30	LRCS1N	O	ROM chip select 1 (even address)
31	XDEC0N	I	ROM BANK #0 select
32	XDECRN	I	ROM BANK #1,#2 select
33	ADECRN	O	decoded upper address for memory
34	WEL	O	write enable for lower byte
35	WEH	O	write enable for upper byte
36	WMEMRN	O	wide memory read
37	OEL0	O	RAM output enable #0 and refresh (even)
38	OEL1	O	↑ #1 ↑
39	OEL2	O	↑ #2 ↑
40	OEL3	O	↑ #3 ↑

Pin number	Signal name	I/O	Remarks
41	OELH4	O	RAM output enable #4 and refresh (even)
42	OELH5	O	↑ #5 ↑
43	OELH6	O	↑ #6 ↑
44	OELH7	O	↑ #7 ↑
45	CELH0	O	RAM chip enable #0 (even address)
46	CELH1	O	↑ #1
47	CELH2	O	↑ #2
48	CELH3	O	↑ #3
49	CELH4	O	↑ #4
50	CELH5	O	↑ #5
51	CELH6	O	↑ #6
52	CELH7	O	↑ #7
53	Vdd (+5V)	P	power supply
54	OEH0	O	RAM output enable #0 and refresh (odd)
55	OEH1	O	↑ #1 ↑
56	OEH2	O	↑ #2 ↑
57	OEH3	O	↑ #3 ↑
58	OEH4	O	↑ #4 ↑
59	OEH5	O	↑ #5 ↑
60	OEH6	O	↑ #6 ↑
61	OEH7	O	↑ #7 ↑
62	* *		no use
63	* *		no use
64	* *		no use
65	CEH0	O	RAM chip enable #0 (odd address)
66	CEH1	O	↑ #1
67	CEH2	O	↑ #2
68	CEH3	O	↑ #3
69	CEH4	O	↑ #4
70	CEH5	O	↑ #5
71	CEH6	O	↑ #6
72	CEH7	O	↑ #7
73	AB0	I	address bit 0 (LSB)
74	Vss (GND)	P	ground
75	AB15	I	address bit 15 from CPU
76	ADD16	I/O	latched upper address bus
77	ADD17	I/O	↑
78	ADD18	I/O	↑
79	ADD19	I/O	↑
80	UBENB	I/O	latched Upper Byte Enable

SLA6170F1M (Gate Array #2) Function Diagram

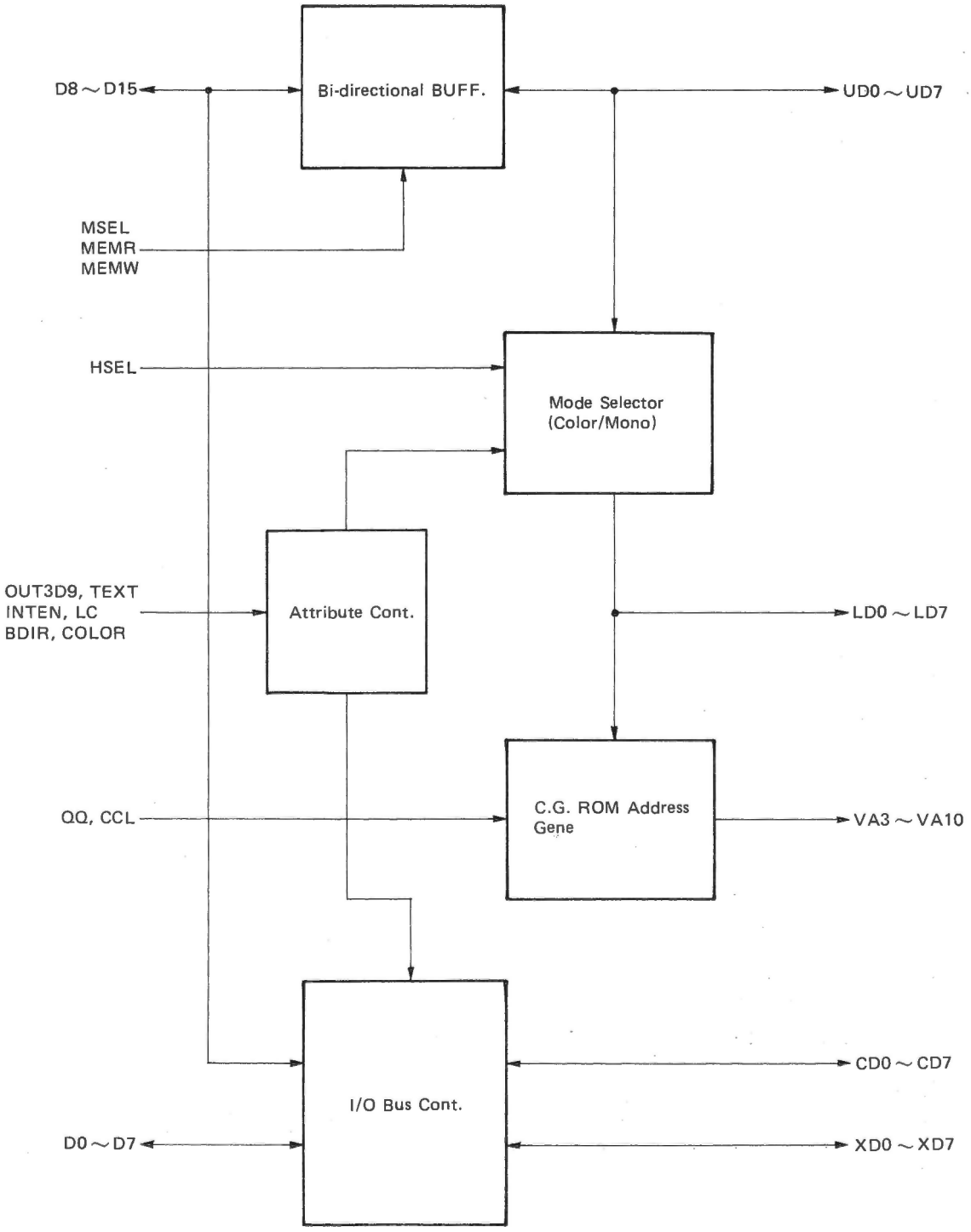


2.12.3 SLA6170F1J (Gate Array #3) Pin Assignment

Pin number	Signal name	I/O	Remarks
1	XD0	I/O	8bits data bus for I/O devices
2	HIGHR	I	"H" when bit 3 is ON in Grafics mode.
3	A0	I	address bit 0 (LSB)
4	D15	I/O	16bits data bus for I/O devices
5	D14	I/O	↑
6	D13	I/O	↑
7	D12	I/O	↑
8	D11	I/O	↑
9	D10	I/O	↑
10	D9	I/O	↑
11	D8	I/O	↑
12	Vss	P	Ground
13	Vdd	P	Power supply
14	D7	I/O	16bits data bus for I/O devices
15	D6	I/O	↑
16	D5	I/O	↑
17	D4	I/O	↑
18	D3	I/O	↑
19	D2	I/O	↑
20	D1	I/O	↑
21	D0	I/O	↑
22	INTA	I	interrupt acknowledge
23	WIOR	I	wide I/O read
24	XB	I	video RAM data enable
25	VA10	O	CG ROM address
26	VA9	O	↑
27	VA8	O	↑
28	VA7	O	↑
29	VA6	O	↑
30	VA5	O	↑
31	VA4	O	↑
32	VA3	O	↑
33	UBE	I	upper byte enable
34	MSEL	I	decoded upper address bit
35	MEMR	I	memory read
36	MEMW	I	memory write
37	CD7	I/O	data bus between CPU and LCD controller
38	CD6	I/O	↑
39	CD5	I/O	↑
40	CD4	I/O	↑

Pin number	Signal name	I/O	Remarks
41	CD3	I/O	data bus between CPU and LCD controller
42	CD2	I/O	↑
43	CD1	I/O	↑
44	CD0	I/O	↑
45	LCDC	I	LCD controller chip select
46	TEXT	I	"H" when in TEXT mode
47	OUT3D	I	"H" when CPU outputs data to 3D9h
48	INTEN	I	"H" when intensity bit is enable
49	QQ	O	for output itensified font
50	CCL	I	clock to latch adress of CG ROM
51	LC	I	"L" when screen device is LCD
52	Vss(GND)	P	ground
53	Vdd(+5V)	P	power supply
54	LD07	I/O	data bus of lower VRAM
55	LD06	I/O	↑
56	LD05	I/O	↑
57	LD04	I/O	↑
58	LD03	I/O	↑
59	LD02	I/O	↑
60	LD01	I/O	↑
61	LD00	I/O	↑
62	BDIR	I	to control data bus between CPU and LCDC
63	COLOR	I	"H" when LCDC is COLOR mode
64	HSEL	I	upper VRAM select
65	UD7	I/O	data bus of upper VRAM
66	UD6	I/O	↑
67	UD5	I/O	↑
68	UD4	I/O	↑
69	UD3	I/O	↑
70	UD2	I/O	↑
71	UD1	I/O	↑
72	UD0	I/O	↑
73	INVLC	O	inverted No.51pin
74	XD7	I/O	8bits data bus for I/O devices
75	XD6	I/O	↑
76	XD5	I/O	↑
77	XD4	I/O	↑
78	XD3	I/O	↑
79	XD2	I/O	↑
80	XD1	I/O	↑

SLA6170F1J (Gate Array #3) Function Diagram

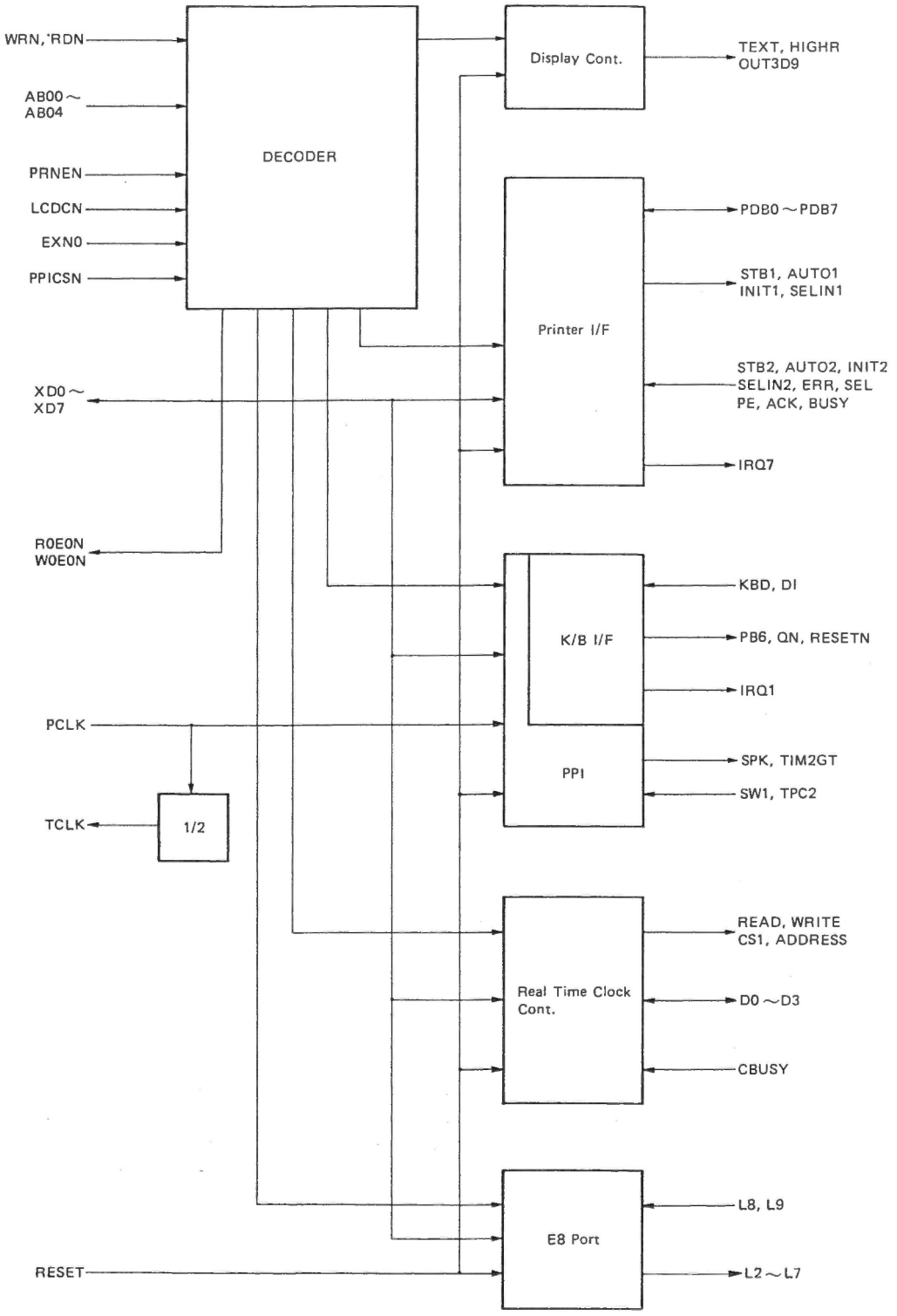


2.12.4 SLA6170F1L (Gate Array #4) Pin Assignments

Pin number	Signal name	I/O	Remarks
1	V s s (GND)	P	ground
2	P C L K	I	2.38MHz
3	T 1 M 2 G T	O	gating timer counter 2
4	X D 7	I/O	8bits data bus for I/O devices
5	X D 6	I/O	↑
6	X D 5	I/O	↑
7	X D 4	I/O	↑
8	X D 3	I/O	↑
9	X D 2	I/O	↑
10	X D 1	I/O	↑
11	X D 0	I/O	↑
12	V s s (GND)	P	ground
13	S P K	O	output to speaker
14	R E S E T N	O	reset to keyboard
15	H I G H R	O	"H" when bit 3 is ON in graphics mode
16	A B 0 4	I	address bus for I/O devices
17	A B 0 3	I	↑
18	A B 0 2	I	↑
19	A B 0 1	I	↑
20	A B 0 0	I	↑
21	P P I C S N	I	parallel I/F chip select
22	W R N	I	I/O write
23	R D N	I	I/O read
24	R E S E T	I	reset for I/O devices
25	V d d (+5V)	P	power supply
26	I R Q 1	O	interrupt request #1
27	P B 6	O	parallel I/F port B bit 6 for K/B control
28	K B D	I	key board data
29	D I	I	key board data enable
30	Q N	O	data to sub CPU on the keyboard
31	P R N E N	I	printer enable
32	P D B 7	O	data bus for output to printer
33	P D B 6	O	↑
34	P D B 5	O	↑
35	P D B 4	O	↑
36	P D B 3	O	↑
37	P D B 2	O	↑
38	P D B 1	O	↑
39	P D B 0	O	↑
40	S T B 1	O	strobe to control printer data

Pin number	Signal name	I/O	Remarks
41	AUTO1	O	auto feed (printer)
42	INIT1	O	initialize (printer)
43	SELIN1	O	enable to output data to printer
44	STB2	I	to sense STB
45	AUTO2	I	to sense AUTO
46	INIT2	I	to sense INIT
47	SELIN2	I	to sense SELIN
48	ERR	I	to sense Error from printer
49	SEL	I	printer select
50	PE	I	to sense paper end
51	ACK	I	"L" when printer recieved data
52	BUSY	I	printer busy
53	Vdd(+5V)	P	power supply
54	IRQ7	O	interrupt request #7
55	EXN0	I	enables port E0h,E4h,E8h
56	R0E0N	O	enables read from port E0h
57	W0E0N	O	enables write to port E0h
58	TEXT	O	"H" when in TEXT mode
59	OUT3D9	O	"H" when CPU output data to 3D9h
60	CS1	O	real time clock chip select
61	TCLK	O	1.19MHz for Timer counter
62	LCDCN	I	LCD controller chip select
63	SW1	I	position of CONFIG SW1. "H" when Test mode
64	TPC2	I	output of timer counter #2 for speaker
65	READ	O	Data read (real time colck)
66	ADDRES	O	address (real time colck)
67	WRITE	O	data write (real time clock)
68	D3	I/O	data bus (real time clock)
69	D2	I/O	↑
70	D1	I/O	↑
71	D0	I/O	↑
72	CBUSY	I	real time clock busy
73	L2	O	PS board control bit
74	L3	O	no use
75	L4	O	no use
76	L5	O	no use
77	L6	O	power control bit for LCD panel (+5V)
78	L7	O	power control bit for LCD panel (-15V)
79	L8	I	position of power SW. "H" when SW is ON.
80	L9	I	bit to sense LOW POWER

SLA6170F1L (Gate Array #4) Function Diagram

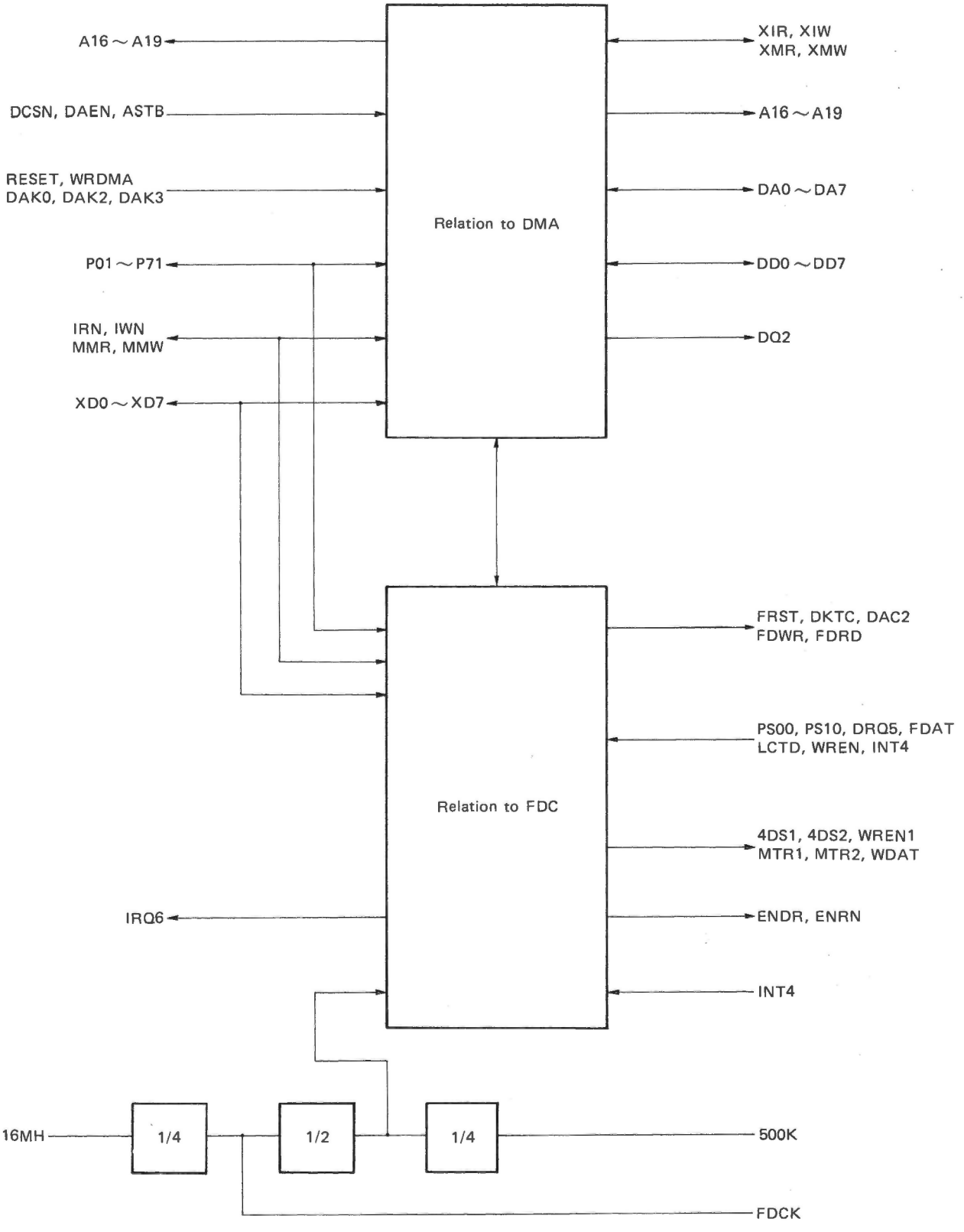


2.12.5 μPD65013-096 (Gate Array #5) Pin Assignment

Pin number	Signal name	I/O	Remarks
1	MMR	I/O	memory read
2	MMW	I/O	memory write
3	IRN	I/O	I/O read
4	IWN	I/O	I/O write
5	* *		no use
6	AEN	I	address enable from CPU
7	XD7	I/O	8bits data bus for I/O devices
8	XD6	I/O	↑
9	XD5	I/O	↑
10	XD4	I/O	↑
11	XD3	I/O	↑
12	XD2	I/O	↑
13	XD1	I/O	↑
14	XD0	I/O	↑
15	GND	P	ground
16	UBE	I	Upper Byte Enable
17	A19	O	Upper address bus (to output when in DMA)
18	A18	O	↑
19	A17	O	↑
20	A16	O	↑
21	A15	O	no use
22	A14	O	no use
23	A13	O	no use
24	A12	O	no use
25	A11	O	no use
26	A10	O	no use
27	A9	O	no use
28	A8	O	no use
29	P71	I/O	lower 8bit address bus
30	P61	I/O	↑
31	P51	I/O	↑
32	P41	I/O	↑
33	P31	I/O	↑
34	P21	I/O	↑
35	P11	I/O	↑
36	P01	I/O	↑
37	DCSN	I/O	DMA controller chip select
38	DAEN	I/O	address enable when in DMA
39	ASTB	I/O	to latch upper 8bits address when in DMA
40	GND	P	ground
41	Vdd (+5V)	P	power supply
42	DD7	I/O	data bus for register of DMA controller
43	DD6	I/O	↑
44	DD5	I/O	↑
45	DD4	I/O	↑
46	DD3	I/O	↑
47	DD2	I/O	↑
48	DD1	I/O	↑
49	DD0	I/O	↑
50	EOP	I	indicates the end of DMA

Pin number	Signal name	I/O	Remarks
51	REST	I	system reset
52	DAK2	I	DMA acknowledge channel 2 for FD controller
53	DAK3	I	DMA acknowledge channel 3
54	WRDMA	O	enable data bus to write to I/O when in DMA
55	DA7	I	transfer address bus when in DMA
56	DA6	I	↑
57	DA5	I	↑
58	DA4	I	↑
59	DA3	I/O	transfer address bus when in DMA and
60	DA2	I/O	address bus for register of DMA controller
61	DA1	I/O	
62	DA0	I/O	
63	FRST	O	reset for floppy disk controller
64	FDCK	O	4MHz for floppy disk controller
65	16MH	I	input from 16MHz oscirator
66	GND		ground
67	500K	O	pulse to transfer data when FDC writes
68	ENRN	O	enables buffer to floppy disk drive (FDD)
69	FDCS	O	chip select of floppy disk controller
70	DAC2	O	DMA acknowledge channel 2 for FD controller
71	FDWR	O	write data to floppy disk by DMA
72	FDRD	O	read data from floppy disk by DMA
73	4DS2	O	floppy disk drive select #2 (B drive)
74	4DS1	O	floppy disk drive select #1 (A drive)
75	MTR1	O	floppy disk drive Motor #1 ON (A drive)
76	MTR2	O	floppy disk drive motor #2 ON (B drive)
77	WDAT	O	data towrite to floppy disk
78	* *		no use
79	DQ2	O	DMA request channel 2 for foppy disk drive
80	IRQ6	O	interrupt request #6
81	LCTD	I	position of R/W head and direction of seek
82	INT4	O	interrupt request #4
83	WREN1	O	enables write data to FDD
84	DKTC	O	indicates the end of data transfer to FDC
85	DRQ5	I	DMA request from FD controller
86	PS00	I	input from FDC. pre-shift at MFM mode
87	PS10	I	
88	WREN	I	indicates to write to FDD
89	FDAT	I	write data to FDD
90	GND		ground
91	Vdd(+5V)		power supply
92	ENDR	O	enables buffer to EXT-FDC connector
93	LCDRDY	I	WAIT to CPU when LCD controller is active
94	DAK0	I	DMA acknowledge channel 0 for memory refresh
95	DMCK	I	clock for DMA controller (4.77MHz)
96	DWAT	O	WAIT to DMA controller
97	XIR	I/O	read from I/O devices and register of DMAC
98	XIW	I/O	write to I/O devices and register of DMAC
99	XMR	I	read from memory when in DMA
100	XMW	I	write to memory when in DMA

μPD65013G-096 (Gate Array #5) Function Diagram



2.13 Liquid Crystal Display (LCD)

As the standard display unit the MultiSpeed employs an LCD (liquid crystal display). This LCD is of the dot matrix type that has 640 x 200 picture elements (pels) so as to display 25 lines x 80 characters on the screen.

If an optional cathode-ray tube (CRT) is connected to the MultiSpeed body, the operator can select either the CRT or the LCD as a monitor. The operator, however, cannot use the LCD and the connected CRT at the same time.

2.14 Liquid Crystal Display (LCD) Controller

As the LCD controller the MultiSpeed employs the V6355D-F LCD controller. This LCD controller, which can control both the LCD and a CRT, is provided with a built-in register bank for function expansion as well as some of the MC6845's built-in registers, and the built-in peripheral circuit of the IBM PC color display adapter which are given for the purpose of providing software compatibility with IBM PCs (personal computers).

This LCD controller supports 1024 character codes stored in the four character font memory areas by using the 16K-byte video memory area which starts from address B8000(hex).

These four character font memory areas are resident in the character generator-ROM (CG-ROM); different areas

store different character fonts. These character fonts are the general character set normal font, general character set bold font, VT-100 dedicated character set normal font, and VT-100 dedicated bold font. The VT-100 dedicated character set is used to emulate the VT-100 by using application programs.

The LCD controller display operation modes are roughly divided into the alphanumeric mode and the graphics mode, each of which is further divided based on the display feature (resolution) to provide a total of five modes supported, as follows:

- o Alphanumeric mode
  - · 40 x 25 character display
  - · 80 x 25 character display
- o Graphics mode
  - · 160 x 200 pels 8-color display (low-resolution display)
  - · 320 x 200 pels 4-color display (medium-resolution display)
  - · 640 x 200 pels monochromatic display (high-resolution display)

This LCD controller supports two types of cursors: text cursor and sprite cursor.

The text cursor comes in a rectangle whose width can be given as desired within a 8 x 8 pels character box; the width is set by both R10 and R11 data out of 6845-registers.

The sprite cursor may come in a desired shape within a range of 16 x 16 pels and also can move continually in dot units on the screen. In addition, the sprite cursor is capable of setting two patterns: one in which the logical product of its own display and another screen display is indicated on the screen and another in which the exclusive logical sum of them is indicated on the screen.

The sprite cursor can be used in both alphanumeric mode and graphic mode, whereas the text cursor can be used only in alphanumeric mode.

This LCD controller has built-in registers called palettes in the register bank so as to specify desired colors. The palette register consists of 16 words, being able to store the 9-bit color code for each palette. A desired color on display can be given by indirectly specifying the corresponding color code stored in the palette register by specifying the corresponding color code. With this function, the MultiSpeed can select 16 colors out of 512 and display them on the screen. Desired colors can be set to desired palette registers, so that the operator can instantly switch the existing color to a desired one without flickering of the display.

These palette registers have been preset in such a way that they give the same color as the IBM PCs when the system is reset by the reset switch mounted on the rear panel of the MultiSpeed, as shown in Fig. 3.14.1 below.

Fig. 2.14.1 Palette registers set value upon presetting

Palette code				Color name	Color code								
I	R	G	B		R_2	R_1	R_0	G_2	G_1	G_0	B_2	B_1	B_0
0	0	0	0	Black	0	0	0	0	0	0	0	0	0
0	0	0	1	Blue	0	0	0	0	0	0	1	0	0
0	0	1	0	Green	0	0	0	1	0	0	0	0	0
0	0	1	1	Cyan	0	0	0	1	0	0	1	0	0
0	1	0	0	Red	0	1	1	0	0	0	0	0	0
0	1	0	1	Magenta	1	0	0	0	0	0	1	0	0
0	1	1	0	Brown	1	0	0	1	0	0	1	0	0
0	1	1	1	White	1	0	0	1	0	0	1	0	0
1	0	0	0	Gray	0	0	1	0	0	1	0	0	1
1	0	0	1	Light Blue	0	0	0	0	0	0	1	1	0
1	0	1	0	Light Green	0	0	0	1	1	0	0	0	0
1	0	1	1	Light Cyan	0	0	0	1	1	0	1	1	0
1	1	0	0	Light Red	1	0	1	0	0	0	0	0	0
1	1	0	1	Light Magenta	1	1	0	0	0	0	1	1	0
1	1	1	0	Yellow	1	1	0	1	1	0	0	0	0
1	1	1	1	White (High intensity)	1	1	1	1	1	1	1	1	1

.If the palette registers have been set as shown in the above table, the 4-bit palette code which specifies palettes may logically be considered to consist of the intensity (I), red (R), green (G), and blue (B) bits. That is, the operator can combine the R, G, and B bits to select the desired eight colors and, moreover, use the I bit to switch those colors to either of two intensities.

This method of specifying colors with palettes is used in all display modes.

On the LCD screen, the MultiSpeed's LCD controller converts colors to eight stages of color shades (intensities), then displays them. The correspondence between specified colors and intensities on the LCD can be found by the following formula:

$$
\begin{array}{rccccc}
 & & & R_2 & R_1 & R_0 \\
 & & & & & R_2 \\
 & & & & B_2 & B_1 \\
+) & & G_2 & G_1 & G_0 & G_2 \\
\hline
 & Y_4 & Y_3 & Y_2 & Y_1 & Y_0
\end{array}
$$

Out of the five bits obtained above, the MultiSpeed's LCD controller uses three bits, Y1 through Y3, to determine intensity.

* Alphanumeric mode

The size of characters displayed in alphanumeric mode is not larger than an 8 x 8 pels character box. However, the size of one pel on the 40 x 25 characters display is the same as that of 2 x 1 pels on the 80 x 25 characters screen.

In the alphanumeric mode the LCD controller uses character codes written in the start 4K-byte area of the video memory area which starts from address B8000(hex) to read out the corresponding character font of the CG-ROM, then indicates the character pattern on display according to the attribute specified for each character.

Both the attribute and the character code of each character occupy one byte each in the text area, so that each character requires two bytes for display: an attribute byte and a character code byte. Fig. 2.14.2 shows the bit configuration of both the character code byte and the attribute byte.

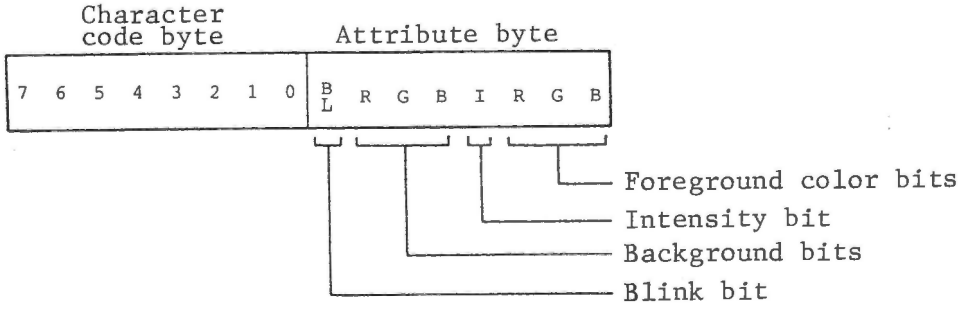


Fig. 2.14.2 Character code byte and attribute byte

The character code byte is fed as the high-order bit of CG-ROM addresses to the CG-ROM together with the three low-order bits generated by the LCD controller, so that desired characters can be displayed.

The attribute byte, on the other hand, carries information on the foreground color, intensity, background color, and blink, which all concern character display.

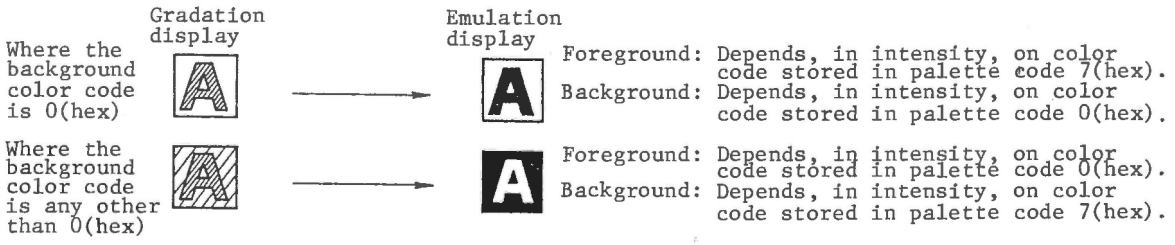
Four foreground color and intensity bits are used as the code to specify the color of characters to be displayed using the palette code, so that 16 colors out of 512 ones can be selected at a time.

Likewise, as many as eight background colors can be specified at a time by use of the 3-bit code. The blink bit is used to specify whether the foreground is to blink or not; if the intra-LCD controller mode register disables the blink function, however, the blink bit of the attribute byte is changed to the intensity (I) bit for the background color, so that 16 colors can be specified as the background color, as in the case of the foreground.

In alphanumeric mode the operator can provide eight gradation stages of display and also the following different display of color display-specified characters on the LCD screen.

If the attribute byte for display characters specifies any color other than black (color code 0(hex)) as the

background color, those characters can be displayed in reversed color on the screen. The background intensity for these reversed characters depends on the color code stored in palette code 7(hex) and the foreground intensity, on the color code stored in palette code 0(hex). If the attribute byte for display characters specifies black as the background color, on the other hand, these characters are displayed on a screen on which the intensity of the foreground and background depend on the color code stored in palette codes 7(hex) and 0(hex) respectively. This display mode is effective a case in which characters are hard to identify on the gradation display screen.



This display mode can be switched to or from the gradation display mode by using the MultiSpeed application program "Setup" or by setting or resetting bit 6 of I/O address E0(hex).

If, also, the attribute byte for display characters has its intensity bit set to 1, those characters can be displayed

bold. This display is effective for both the CRT display and the LCD.

This display mode can be switched to or from the general display mode by using the MultiSpeed application program "Setup" or by setting or resetting bit 5 of I/O address E0(hex).

The above-mentioned two special display modes can be set at the same time.

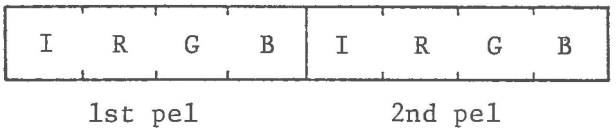
* Graphics mode

The graphics mode comes in three types, depending on the display feature (resolution): 160 x 200 pels graphics, 320 x 200 pels graphics, and 640 x 200 pels graphics.

In every one of these three graphics modes the text cursor is disabled but the sprite cursor is enabled in use.

o 160 x 200 pels graphics mode

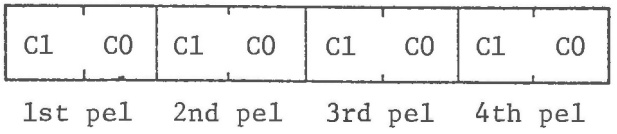
In this mode each dot size is equal to the size of 4 x 1 pels in the 640 x 200 pels graphics mode. Each picture element (pel) uses four bits of the video memory area and is capable of setting 16 colors.



Format in video memory

o 320 x 200 pels graphics mode

In this mode each pel size is equal to the size of 2 x 1 pels in the 640 x 200 pels graphics mode. Each pel uses two bits of video memory area and is capable of setting four colors.



In the 320 x 200 pels graphics mode the color can be selected by activating either of the two color palette groups SET 1 and SET 2 so as to specify the palette of the activated group by using two bits, C1 and C0. The SET 1 and SET 2 groups can be selected by bit 5 of the intra-LCD controller color selection register in such a way that if bit 5 is set to 0 or 1, the SET 1 or SET 2 group is selected respectively. If, in this case, the monochromatic display mode is specified, both the Set 1 and SET 2 groups provide the same contents. If bits C1 and C0 are both set to 0, the background color is selected by four bits, bits 0 through 3, of the color selection register. Fig. 2.14.3 outlines display colors in the 320 x 200 pels graphics mode.

Fig. 2.14.3 Outline of 320 x 200 pels graphics mode display colors

C1	C0	Color	SET 1 I	SET 1 R	SET 1 G	SET 1 B	SET 2 I	SET 2 R	SET 2 G	SET 2 B	B & W I	B & W R	B & W G	B & W B
0	0	Back-ground	SEL I	SEL R	SEL G	SEL B	SEL I	SEL R	SEL G	SEL B	SEL I	SEL R	SEL G	SEL B
0	1	Color 1	SEL IN	0	1	0	SEL IN	0	1	1	SEL IN	0	1	1
1	0	Color 2	SEL IN	1	0	0	SEL IN	1	0	1	SEL IN	1	0	0
1	1	Color 3	SEL IN	1	1	0	SEL IN	1	1	1	SEL IN	1	1	1

o 640 x 200 pels graphics mode

In this mode each pel size is equal to the size of 1 x 1 pels. Each pel uses each bit of the video memory area. In this mode, two colors can be displayed in such a way that the video memory area bit which is set appears on display in a color selected by bits 0 through 3 of the color selection register, whereas the bit which is not set appears in the color of color code 0(hex), i.e. black.

* Programming considerations

This LCD controller uses those registers listed in Fig. 2.14.4 below, to set the operation mode, desired functions, etc. and also to read data from or write it to the internal register.

Fig. 2.14.4

Address (hex)	R/W	Usage
3D0	W	6845 Address Register
3D1	R/W	6845 Data Register
3D8	R/W	Mode Control Register
3D9	W	Color Select Register
3DA	R	Status Register
3DD	W	Register Bank Address
3DE	W	Register Bank Data

6845-Address and Data Registers: 3D0(hex) and 3D1(hex)

The registers listed above are used to provide access to the 6845-register built in the LCD controller.

The 6845-address register serves as a pointer for a desired one of the 6845-registers.

The 6845-data register is used to provide access to registers selected by the address register.

Fig. 2.14.5 below gives the 6845-registers built into the LCD controller and their internal addresses.

Fig. 2.14.5 6845-registers

Internal address (hex)	R/W	Usage
0A	W	R10, cursor start scan line address
0B	W	R11, cursor end scan line address
0C	R/W	R12, start address (high)
0D	R/W	R13, start address (low)
0E	R/W	R14, cursor address (high)
0F	R/W	R15, cursor address (low)
10 - 11		not used

Mode Control Register: 3D8(hex)

This register can be accessed in 8-bit units in such a way that in write operation it can be used to set the LCD controller mode and, in read operation, to output this controller's ID number (C0(hex)).

Bit	Usage
7	Stand-by mode setting bit. If this bit is set to 1, the LCD controller enters the stand-by mode.
6, 4	Graphics display resolution selecting bits. These two bits can be combined to select resolutions on graphics display, as listed below.

Bit		Resolution
6	4	
0	0	320 x 200 pels
0	1	640 x 200 pels
1	0	160 x 200 pels
1	1	Not used

5 Blinking function enabling bit. If this bit is set to 1, the character blinking function is validated in the alphanumeric mode. If this bit is set to 0, on the other hand, bit 7 of the attribute byte is used as the intensity bit for the background color.

3 Video signal output suspending bit. The video signal output must be suspended when the mode is changed. Therefore, be sure to set this bit to 1 to suspend the video signal for a certain lapse of time when the mode is switched.

2 Monochromatic/color mode selecting bit. If this bit is set to 1, monochromatic graphics are given on the CRT.

1 Graphic mode selecting bit. If this bit is set to 1 or 0, graphics mode or alphanumeric mode is selected respectively. The resolution in graphics mode can be specified by bits 6 and 4.

0	80 x 25 characters display selecting bit. If this bit is set to 1, the 80 x 25 character display is selected, if it is set to 0, the 40 x 25 character display is selected.

Note here that bits 7 and 6 are write-protected by the lock feature in order to protect their contents from an unexpected write operation. To unlock them, set bit 7 of I/O address 3DD(hex) to 1; to lock them again, set that bit to 0.

The mode control register can be reset by pressing the reset switch.

Color Select Register: 3D9(hex)

This 6-bit register is exclusively used for accessing.

Bit	Usage
7 - 6	Not used
5	This bit selects the color set in the 320 x 200 pels graphics mode, as follows: 0: SET 1 is activated. 1: SET 2 is activated.
4	This bit, if set to 1, selects the high-intensity color set in the 320 x 200 pels graphics mode.

3 - 0 The palette code written to these bits specifies the border color in every display mode. At the same time, the background color in the 320 x 200 pels graphics mode is specified.

The color select register can be reset by pressing the reset switch.

Status Register: 3DA(hex)

Bit	Usage
7 - 5	Not used
4	This bit, if set to 1, indicates that the video dot information (input signal for color palettes) is being output. The low-order two bits of the register bank address are combined as follows to select the desired one of four dots.

Register bank address register bits 1 and 0		Video dot information
0	0	Blue (B)
0	1	Green (G)
1	0	Red (R)
1	1	Intensity (I)

This bit, i.e. bit 4 of the status register, is provided for the purpose of testing. This bit can be used to make sure that the video information is correctly generated and also that the

mode selection register, color selection register, and all other write-dedicated registers are correctly operating.

Bit	Usage
3	This bit, when set to 1, indicates that the system is in the vertical return line period. This bit, in the monochromatic adapter mode, serves as video dot information like bit 4.
2 - 1	Not used
0	This bit, when set to 1, indicates that the display is OFF because of the return line.

Register Bank Address and Data Registers: 3DD(hex) and 3DE(hex)

These two registers are used to access the intra-register bank register built in the LCD controller.

The register bank address register serves as a pointer for each of the intra-register bank registers.

The register bank data register is used to output data to registers selected by the address register.

Fig. 2.14.6 gives the correspondence between the intra-register bank registers and their internal addresses.

Fig. 2.14.6 Intra-register bank registers

Address (hex)	R/W	Usage
0 - 1F	W	Sprite pattern data (S1)
20 - 3F	W	Sprite pattern data (S2)
40 - 41	W	Color palette #0
42 - 43	W	" #1
44 - 45	W	" #2
46 - 47	W	" #3
48 - 49	W	" #4
4A - 4B	W	" #5
4C - 4D	W	" #6
4E - 4F	W	" #7
50 - 51	W	" #8
52 - 53	W	" #9
54 - 55	W	" #10
56 - 57	W	" #11
58 - 59	W	" #12
5A - 5B	W	" #13
5C - 5D	W	" #14
5E - 5F	W	" #15
60 - 61	W	Horizontal sprite position
62 - 63	W	Vertical sprite position
64	W	Test/smooth scroll/sprite display control
65	W	Monitor control
66	W	MONO/LCD control/raster adjustment and control
67	W	Processor, page selection/clock synchronization position control
68	W	Sprite color selection

Sprite Pattern Data Register: Internal addresses
0(hex) to 3F(hex)

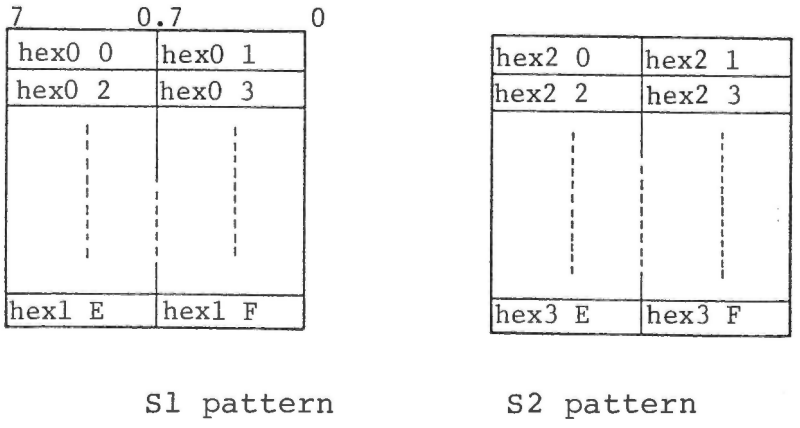
These registers are used to define sprite patterns, being able to store 16 x 16 dots pattern data for both S1 and S2 patterns.

The S1 pattern is AND'ed with other patterns on the screen, whose result is then displayed; the foreground color for this pattern is determined by the intra-register bank sprite color selection register. The background color for this pattern is white (1).

The S2 pattern is exclusive-OR'ed with other patterns on the screen, whose result is then displayed. The foreground color is determined by the sprite color selection register and the background color, transparent.

Fig. 2.14.7 below gives the correspondence between these two patterns and their register data addresses.

Fig. 2.14.7 Sprite pattern data



S1 pattern S2 pattern

Color Palette Registers #0 to #15: Internal addresses 40(hex) to 5F(hex)

This register group is of the 16-word x 9-bit configuration and can store 16 9-bit color codes, to select desired colors in all display modes. With this function, the operator can use any desired 16 colors out of the 512 colors.

Fig. 2.14.8 lists the bit configuration for these color palette registers.

Palette #0:

Internal address 41(hex)		40(hex)
* * * * *	R_2 R_1 R_0	* G_2 G_1 G_0 * B_2 B_1 B_0

Palette #1:

Internal address 43(hex)		42(hex)
* * * * *	R_2 R_1 R_0	* G_2 G_1 G_0 * B_2 B_1 B_0

Palette #15:

5F(hex)	5E(hex)

* = Don't care

Fig. 2.14.8 Color palette registers

These color palette registers are so preset as to provide the same color as the IBM PC, each time the reset switch is pressed.

Horizontal Sprite Position and Vertical Sprite Position Registers: Internal addresses 60(hex) to 63(hex)

These registers are used to define the sprite cursor position on the screen, storing its horizontal position and vertical position in internal addresses 60 to 61(hex) and internal addresses 62 to 63(hex) respectively.

The home position of the sprite cursor is the top left cursor corner dot of the pattern; this dot gives the position coordinates of the sprite cursor. As shown in Fig. 2.14.9 below, the sprite cursor position coordinates and the display coordinates are shifted 16 bits from each other both horizontally and vertically.

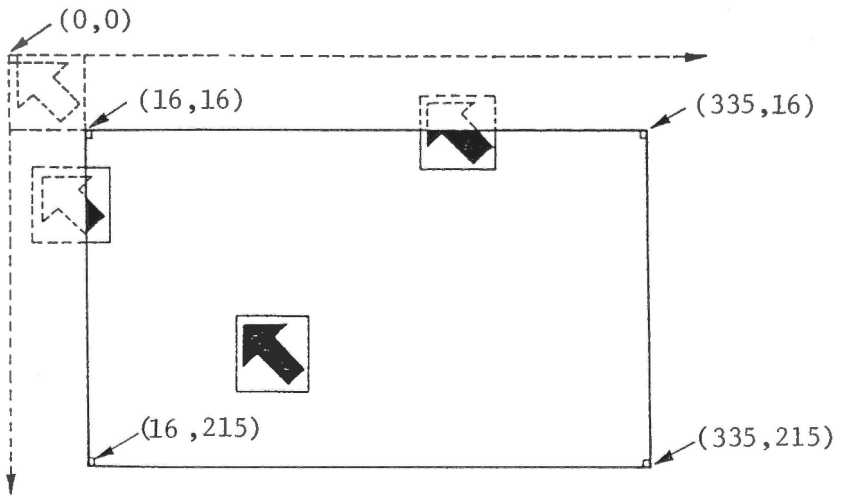


Fig. 2.14.9 Sprite cursor position coordinates and display coordinates

Fig. 2.14.10 below shows the bit configuration of both the horizontal and vertical sprite position registers.

	Internal address 60(hex)	61(hex)
Horizontal sprite position register	* * * * * * * H_8	H_7 H_6 H_5 H_4 H_3 H_2 H_1 H_0

	62(hex)	63(hex)
Vertical sprite position register	* * * * * * * *	V_7 V_6 V_5 V_4 V_3 V_2 V_1 V_0

= Don't care

Fig. 2.14.10 Horizontal and vertical sprite position registers

Test/smooth scroll/sprite display control register:

Internal address 64(hex)

This 8-bit register is exclusively used for the write operation.

Bit	Usage
7 - 6	These two bits, if both set to 1, permits the LCD controller to enter the test mode, inhibiting general operations. These two bits can be reset to 0 by the vertical synchronization signal.
5 - 3	These three bits, if set to 0 or 1, shift up the screen raster line in the alphanumeric mode by as much as their representing number.
2	S2 sprite cursor enable bit. This bit, if set to 1, validates sprite cursor S2.
1	S1 sprite cursor enable bit. This bit, if set to 1, validates sprite cursor S1.
0	Sprite cursor blinking bit. This bit, if set to 1, causes the sprite cursor to start blinking.

This register can be reset to 0 by pressing the reset switch.

Monitor Control Register: Internal address 65(hex)

This 8-bit register is exclusively used for the write operation.

Bit	Usage
7	Not used
6	Set to 1 when S-RAMs are used as video memory and set to 0 when D-RAMs are used. For the MultiSpeed, set this bit to 1.
5	Set to 1 to direct the display contents to the CRT; set to 0 to direct them to the LCD.
4	Set to 0 to connect a color monitor to the body; set to 1 to connect an IBM monochromatic monitor.
3	Set to 1 to connect a PAL/SECAM type monitor to the body; set to 0 to connect an NTSC type monitor.
2	Selects the number of horizontal dots on the display screen, as follows: 0: 640 or 320 dots 1: 512 or 256 dots
1 – 0	Those two bits are used to select the number of vertical lines.

Bit		Usage
1	0	
0	0	192 lines
0	1	200 lines
1	0	204 lines
1	1	64 lines

This register is initialized to 41(hex).

Monochromatic Monitor/LCD Control Register: Internal address 66(hex)

This 8-bit register is exclusively used for the write operation.

Bit	Usage
7	This bit, when set to 1, permits bit 3 of the status register to indicate the video dot information and bit 0 to change to be of horizontal synchronization in order to enable the underline function.
6	This bit, when set to 1, enables monochromatic display and, when set to 0, enables 16-color display.
5 - 4	These two bits are used to select a desired LCD driver shift clock frequency. The MultiSpeed employs the controller selected by these two bits (bits 5 and 4) set to 1 and 0 respectively.

3 - 2	These two bits are used to select a desired LCD driver type. The MultiSpeed employs the controller selected by these two bits (bits 3 and 2) set to 0 and 1 respectively.
1 - 0	These two bits are used to select the number of vertical raster adjustment lines employed on the upper half of the LCD screen. The MultiSpeed gives such a number of lines as to be determined by these two bits (bits 1 and 0) both reset to 0.

In the MultiSpeed this register is initialized to 24(hex).

Configuration Mode Register: Internal address 67(hex)

This 8-bit register is exclusively used for write operation.

Bit	Usage
7	This bit, when set to 1, enables bus operation by the 16-bit processor.
6	Not used
5	Used to select the AC drive control signal for LCD.
4 - 0	These five bits are used to generate the enable clock (E-CLK) or weight clock (W-CLK) for the LCD driver when the LCD controller is in the

LCD mode. In the CRT mode, these five bits are used to adjust the horizontal display position in a range of dot numbers -7 through 8.

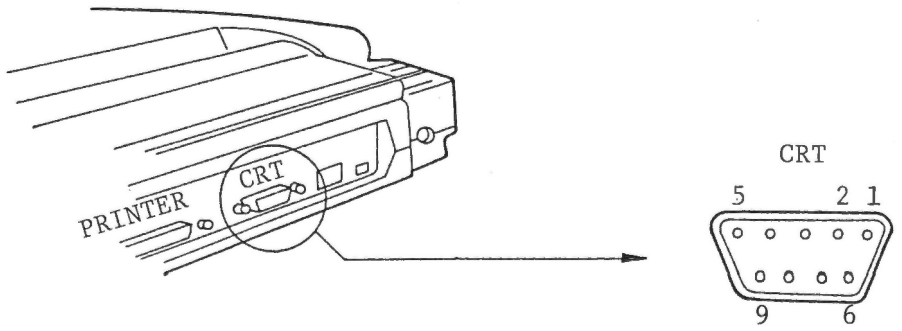
Sprite Cursor Color Selection Register: Internal address 68(hex)

This 8-bit write operation-dedicated register is used to select the foreground color of the two sprite cursors, using palette codes, as follows.

Bit	Usage
7 – 4	Used to select the foreground color of the S2 sprite cursor.
3 – 0	Used to select the foreground color of the S1 sprite cursor.

2.15 CRT Display Interface

The MultiSpeed is provided with a 9-pin connector mounted on its rear panel, for the purpose of connecting a CRT display to it. The MultiSpeed sends only the output signal of the TTL level through this connector. The signal pins of this connector are explained below.



Pin #	Signal name	I/O	Usage
1 — 2	Ground	O	Color display signal
3	Red	O	
4	Green	O	
5	Blue	O	
6	Intensity	O	Intensity signal
7	OR	O	This video signal is a logical sum of the R, G, and B signals and is used in monochromatic display.
8	Horizontal Sync	O	Horizontal synchronization signal
9	Vertical Sync	O	Vertical synchronization signal

2.16 Keyboard and Keyboard Controller

The MultiSpeed keyboard is roughly comprised of the typewriter-type keyboard key group, 10 function keys group, and calculator-type keypad.

The 10 function keys function can be defined by software by each user with the shift key held down or not, to enable setting a total of 20 functions.

The key top of both the Caps Lock key on the typewriter-type keyboard and the Num Lock key on the calculator-type keypad has a built-in LED (light emitting diode), so that the operator can easily understand the ON/OFF status of these two keys.

At the bottom stage on the keyboard the Pop Up key and the Help key are provided marked in red. The Pop Up key is used as the function key to call the Pop Up program, i.e. MultiSpeed application program. The Help key is used to display the information on the operations or functions of the MultiSpeed itself, its application program, etc. These two keys (Pop Up and Help keys) will generate key scan codes that the IBM PC does not, and have their functions fixed by the intra-BIOS routine.

Figs. 2.16.1 and 2.16.2 show the keyboard layout for English-speaking countries and German-speaking countries respectively.

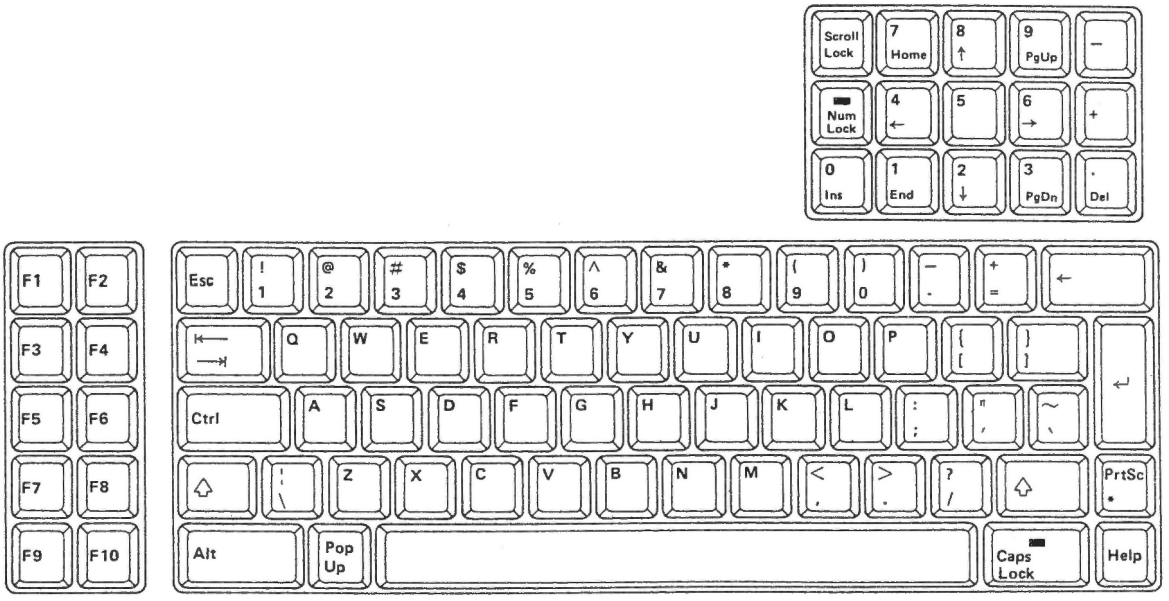


Fig. 2.16.1 English-edition keyboard layout

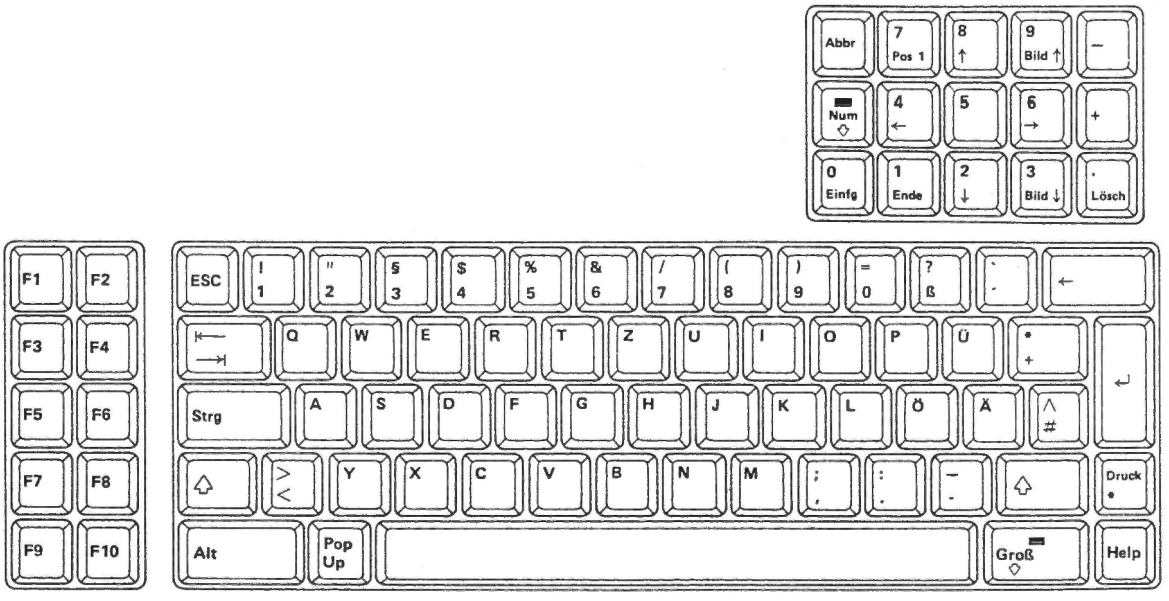


Fig. 2.16.2 German-edition keyboard layout

The MultiSpeed keyboard controller has functions to detect key-in, debounce, typematic, and queue key-in operations.

Immediately after detecting key pressing and releasing, the keyboard controller sets to the intra-controller

first-in-first-out (FIFO) buffer the 1-byte MAKE code and the BREAK code shown in Fig. 2.16.4 before respectively.

The BREAK code is given a sum of 80(hex) and the MAKE code value assigned to each relevant key. The FIFO key-in buffer accommodates 16 times key-in operations, thus enabling queueing key-in operations. If the FIFO key-in buffer overflows, overrun code FF(hex) in set to the dedicated 17th buffer.

This keyboard controller has its own built-in timer because of the typematic function. Immediately after any key is pressed, this timer starts counting and, if the key is held down in excess of 550 ms, generates the MAKE code continually afterward for each 100 ms of time lapse. Fig. 2.16.3 shows the timing chart for typematic operation where two keys are pressed continually.

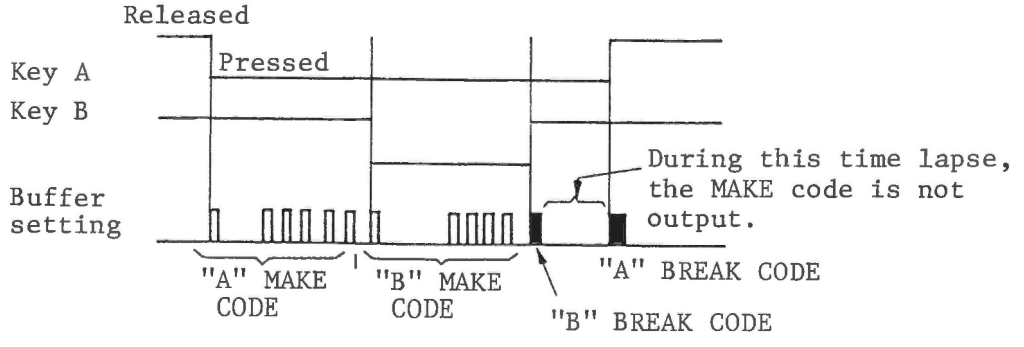
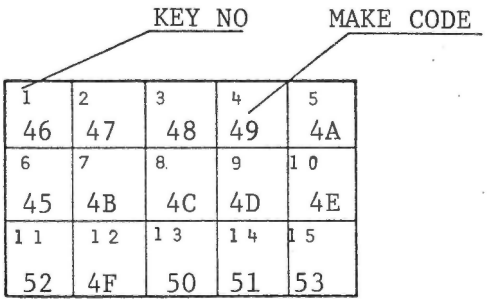


Fig. 2.16.3 Timing chart for typematic operation

The MAKE code stored in the FIFO key-in buffer is transferred by the intra-BIOS routine to the keyboard scan code register of I/O port address 060(hex).

Note: The MAKE codes are all represented in hexa-decimal notation.



16 3B	17 3C	18 01	19 02	20 03	21 04	22 05	23 06	24 07	25 08	26 09	27 0A	28 0B	29 0C	30 0D	31 0E
32 3D	33 3E	34 0F	35 10	36 11	37 12	38 13	39 14	40 15	41 16	42 17	43 18	44 19	45 1A	46 1B	47 1C
48 3F	49 40	50 1D	51 1E	52 1F	53 20	54 21	55 22	56 23	57 24	58 25	59 26	60 27	61 28	62 29	
63 41	64 42	65 2A	66 2B	67 2C	68 2D	69 2E	70 2F	71 30	72 31	73 32	74 33	75 34	76 35	77 36	78 37
79 43	80 44	81 38	82 70	83 39										84 3A	85 7E

Fig. 2.16.4 Make scan code mapping

* Programming considerations

The data to be transferred by BIOS to the keyboard scan code register are converted beforehand to serial data, then transferred using the handshaking protocol. When the data is stored to the keyboard scan code register, BIOS generates hardware interrupt level 1. The data entered

through the keyboard can be used by application programs only after it is stored to this register.

Keyboard Scan Code Register: 060(hex)

This register is used to take in data entered through the keyboard, in MAKE scan codes to application programs.

2.17 Printer Interface

The MultiSpeed is provided with a printer conecting a 25-pin connector mounted on its rear panel. The signal pins of this connector will now be explained. The plus (+) and minus (-) signs immediately preceding the signal name in the table below represent the active level of the relevant signal. I (for input) and O (for output) given in the I/O column give the direction in which the signal is sent as viewed from the connector.

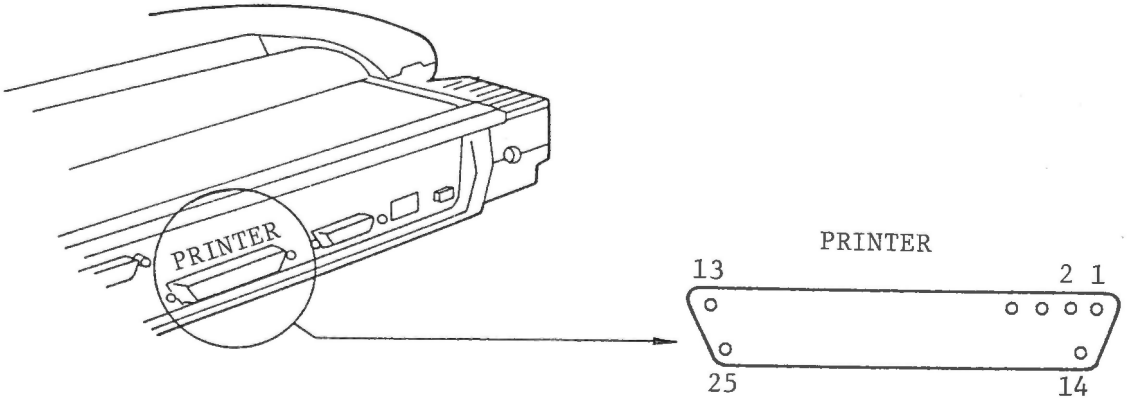


Fig. 2.17.1

Pin #	Signal name	I/O	Usage
1	- Strobe	O	Pulse signal used to latch data 0 through data 7 into printer
2 - 9	+ Data 0 7	O	8-bit parallel data signal
10	- Ac- knowledge	I	Pulse signal which indicates that data are received by printer
11	+ Busy	I	This signal, when set to high level, indicates that the printer is not ready for data reception.
12	+ Paper End	I	This signal, when set to high level, indicates the paper-out status of the printer.
13	+ Select	I	This signal, when set to the high level, indicates that the printer is selected.
14	- Auto Feed	O	This signal, when set to low level, causes the printer to automatically feed one line of print paper immediately after printing the data in progress
15	- Error	I	This signal is set to low level if the printer enters the following: · PAPER END · OFF-LINE state · Error state
16	- Initialize Printer	O	This signal, when set to low level, initializes the printer, clearing the print buffer.
17	- Select Input	O	Only while this signal is at low level, the printer can receive data.
18-25	Ground		

2.18 Power Supply

The power supply is incorporated in the body and feeds five levels of DC potentials (+5V, +12V, -5V, -12V, and -20V) to the corresponding system units.

This power supply actually serves as a DC-to-DC converter, receiving input power from the AC adapter, automobile power adapter and built-in Ni-Cd battery, all of which are DC power sources.

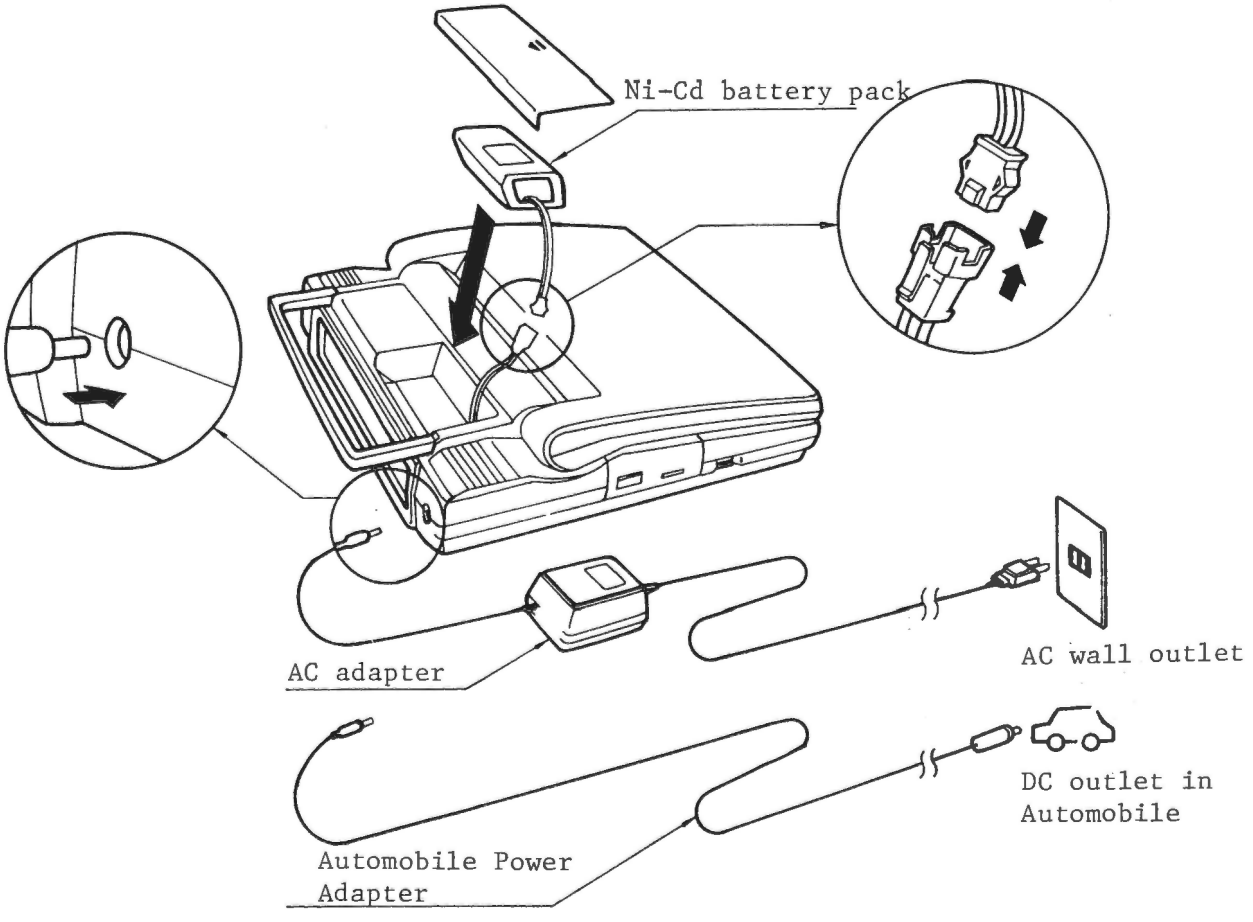


Fig. 2.18.1

2.19 Ni-Cd Battery Pack and Back-up Battery

The MultiSpeed has two built-in Ni-Cd batteries: the main battery pack and the back-up battery.

The main battery pack is used to drive the system when it is not powered from an external source, so this battery pack is always recharged whenever the system is supplied with input power from the AC adapter or automobile power adapter, regardless of whether the POWER switch or the BACK-UP POWER switch is ON or OFF. Moreover, the main battery pack can be detached or replaced, so that the MultiSpeed can be used without the pack as long as it is connected to the AC adapter or automobile power adapter.

The back-up battery is used as a back-up power supply for the realtime clock and some RAMs, and is recharged by the main battery pack or external power supply when the BACK-UP POWER switch is ON.

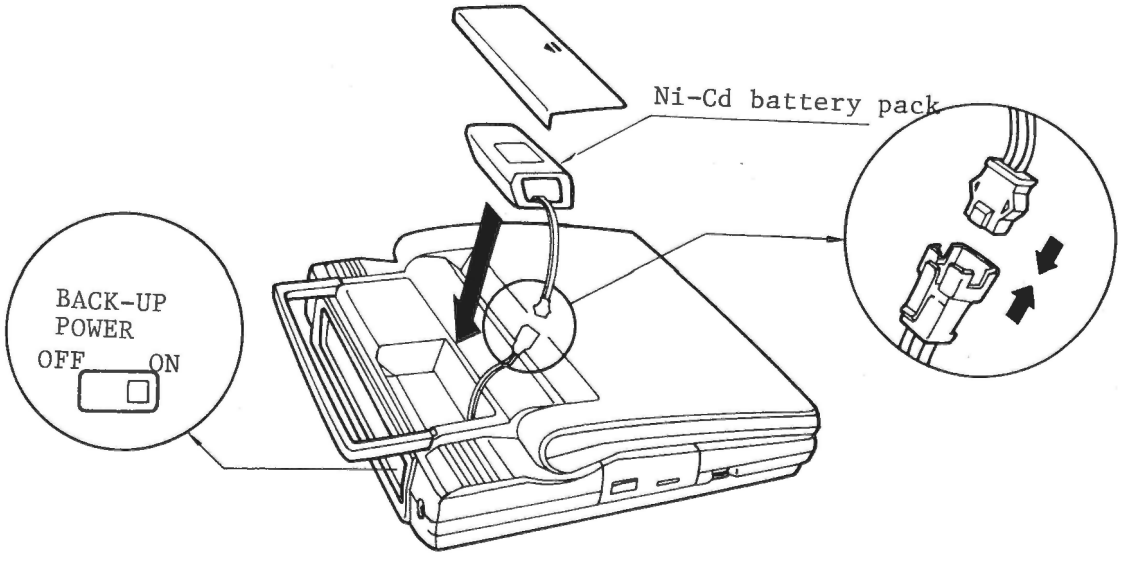


Fig. 2.19.1

2.20 AC Adapter

The AC adapter is used to supply power to the system unit from a wall outlet and also to recharge the built-in Ni-Cd batteries.

3. Option Cables

3.1 Printer Cable

The printer cable can be used to connect a printer to the MultiSpeed. Fig. 3.1.1 shows printer cable pin allocation.

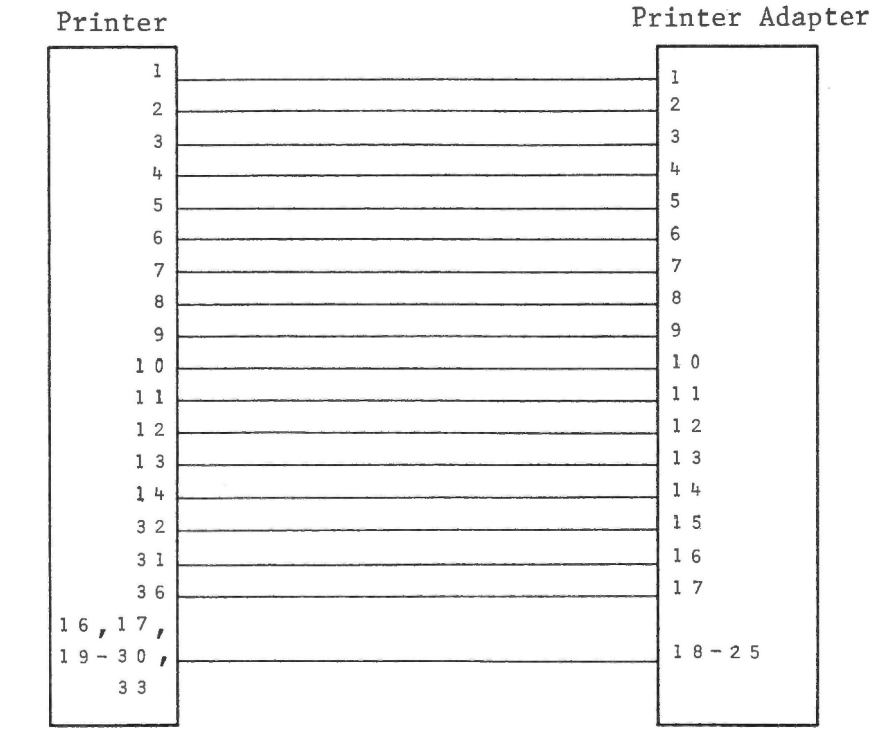


Fig. 3.1.1 Printer cable pin allocation

3.2 RS-232C Cable

The RS-232C cable can be used to connect the MultiSpeed serial adapter with the RS-232C port of other computers or peripheral devices, so that the MultiSpeed can execute asynchronous communication or serial data transfer with them.

The RS-232C cable comes in two types, depending on the device connected to the MultiSpeed. One is the nromal type exclusively used to output data from the MultiSpeed to devices connected to it. The other is the reverse type used for mutual communication between the MultiSpeed and devices connected to it.

Figs. 3.2.1 and 3.2.2 show RS-232C cable pin allocation for the normal type and the reverse type respectively.

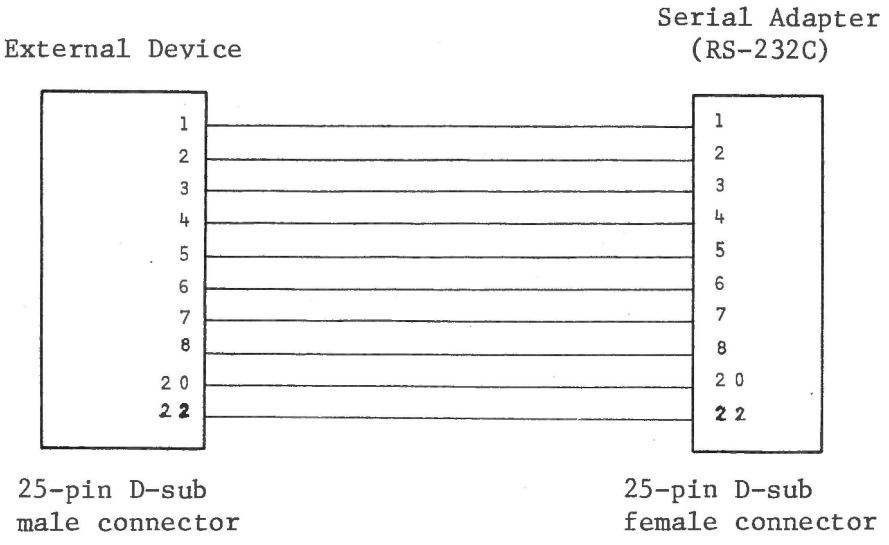


Fig. 3.2.1 RS-232C cable pin allocation (normal type)

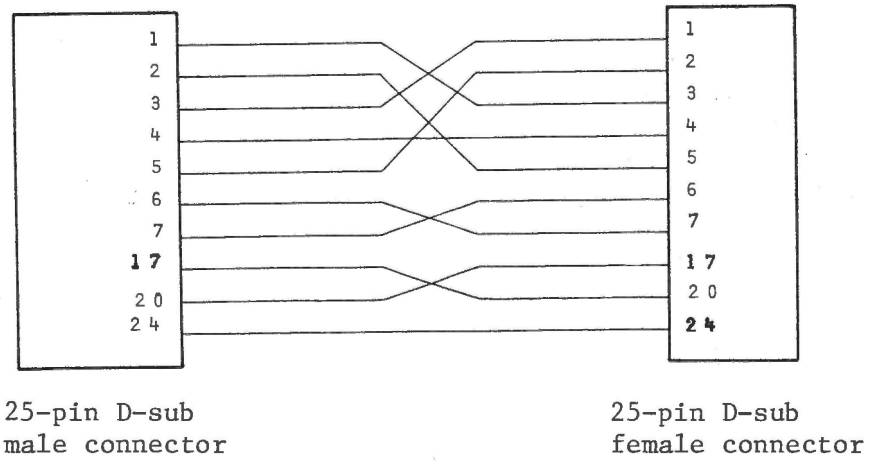


Fig. 3.2.2 RS-232C cable pin allocation (reverse type)

3.3 External FDC Cable

The external FDC cable can be used to connect the MultiSpeed EXT FDC adapter and the IBM personal computer expansion drive adapter. With this, the operator can use the built-in 3.5-inch floppy disk drive of the MultiSpeed as an IBM personal computer expansion drive.

Fig. 3.3.1 shows external FDC cable pin allocation.

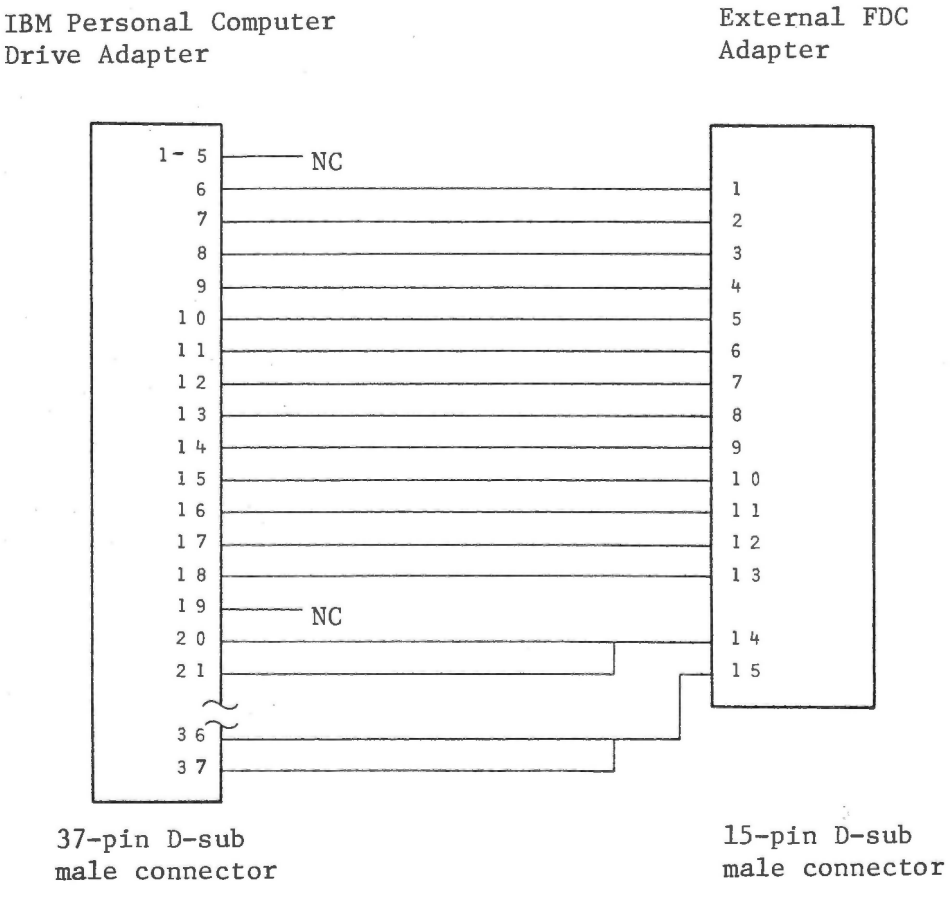


Fig. 3.3.1 External FDC cable pin allocation

3.4 Automobile Power Cable

The automobile power cable is used to supply power to the system unit from an automobile DC outlet. This adapter will also recharge the two built-in Ni-Cd batteries.

Appendix: Logic Timing Diagrams

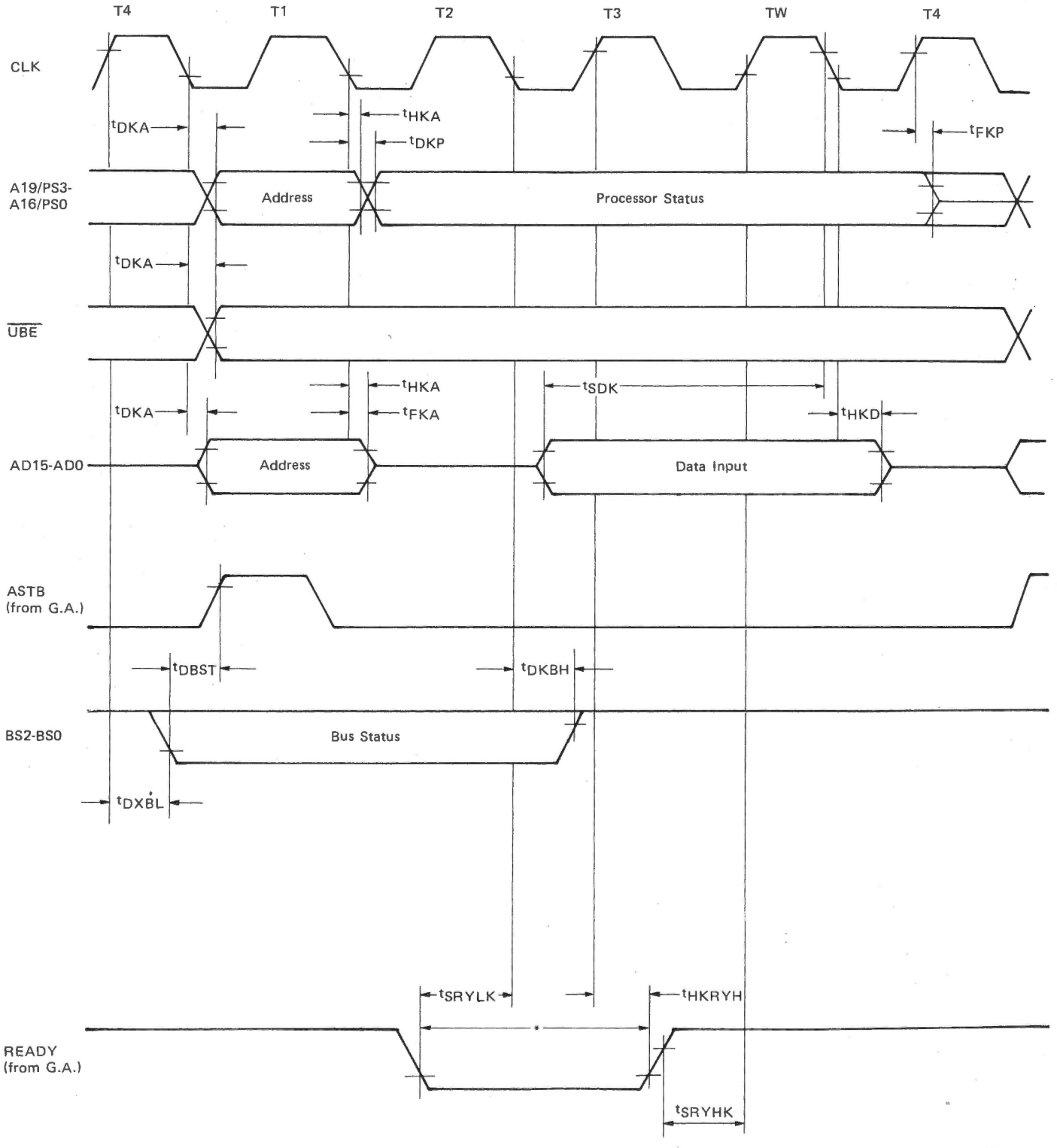
1. CPU Interface
2. DMA Data Transfer Interface
3. Memory Interface
4. LCD Interface

CPU Interface

Pramater	Symbol	Min	Max	Units
System Clock Cycle	t_{CYK}	100	500	ns
Clock pulse High level width	t_{KKH}	41		ns
Clock pulse Low level width	t_{KKL}	49		ns
Clock Rise time	t_{KR}		5	ns
Clock Fall time	t_{KF}		5	ns
READY inactive Setup time from CLK↓	t_{SRYLK}	0		ns
READY inactive Hold time from CLK ↑	t_{HKRYK}	11		ns
READY active Setup time from CLK↓	t_{SRYHK}	t_{KKL} -10		ns
Data Setup time from CLK↓	t_{SDK}	10		ns
Data Hold time from CLK ↑	t_{HKD}	10		ns
Imput Fall time (except CLK)	t_{IF}		12	ns
Output Rise time	t_{OR}		20	ns
Output Fall time	t_{OF}		12	ns
CLK →Address Dilay time	t_{DKA}	10	48	ns
CLK →Address Hold time	t_{HKA}	10		ns
CLK ↓→PS Dilay time	t_{DKP}	10	50	ns
CLK ↓→PS floating Dilay time	t_{FKP}	10	50	ns
CLK ↓→Address floating Dilay time	t_{FKA}	t_{HKA}	50	ns
BS↓→ASTB↑ Dilay time	t_{DBST}		20	ns
CLK ↓→BS↓Dilay time	t_{DKBL}	10	50	ns
CLK ↑→BS↑Dilay time	t_{DKBH}	10	50	ns
CLK ↓→Data output Dilay time	t_{DKD}	10		ns
CLK ↓→Data float Dilay time	t_{FKD}	10		ns

CPU Interface

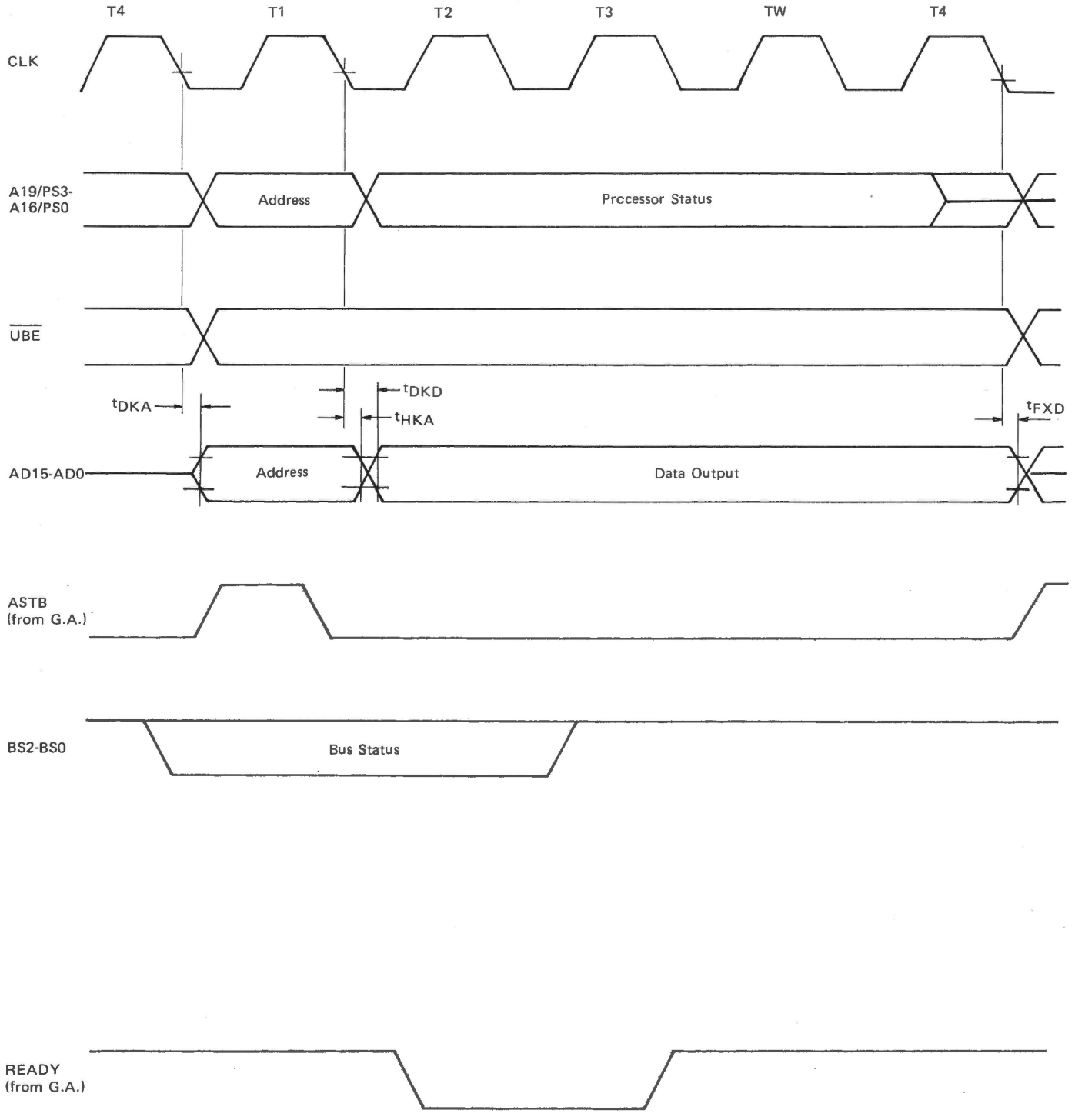
Read Cycle



*: During this period the Ready signal must be fixed to the low level (or high level).

CPU Interface

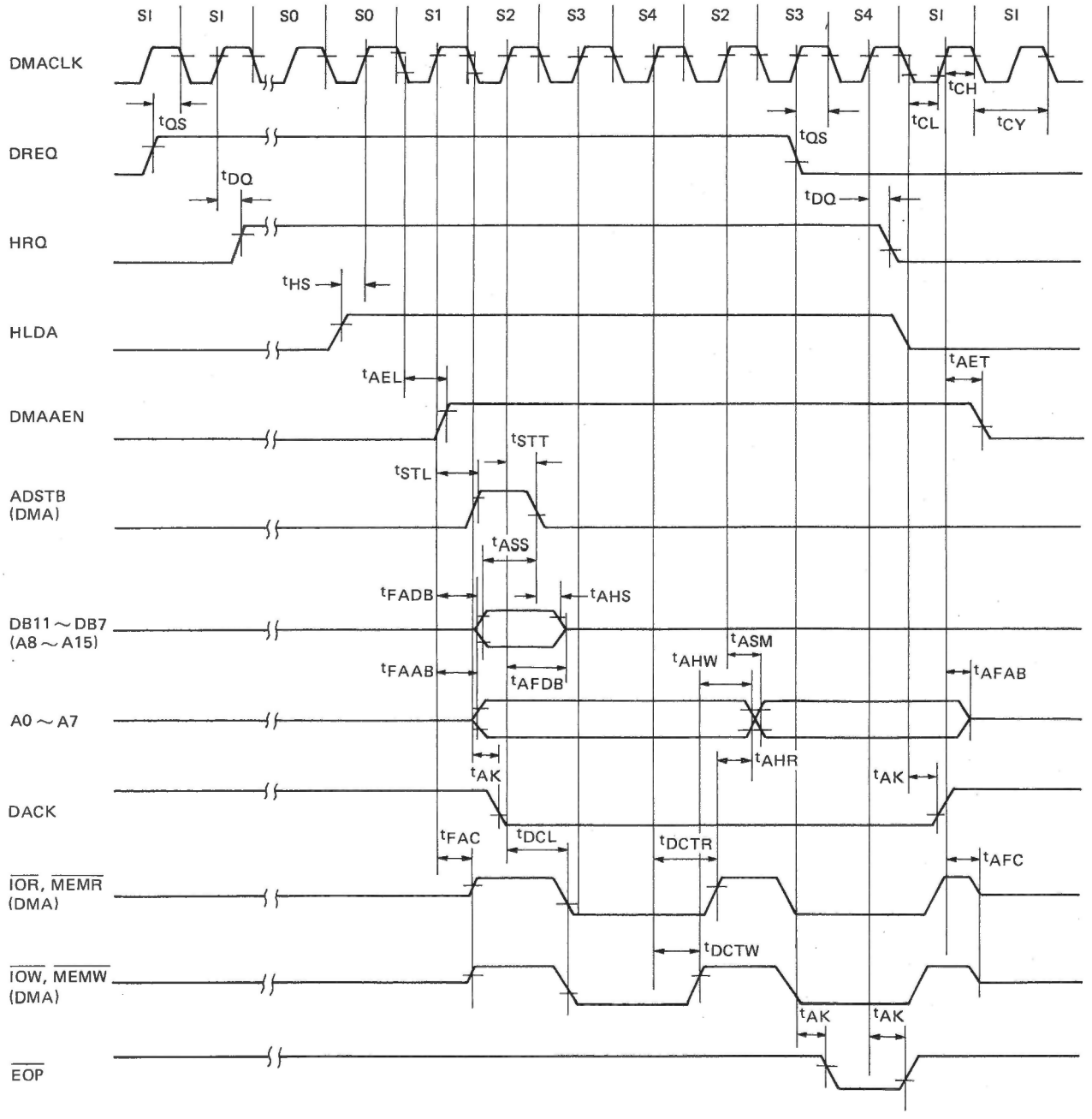
Write Cycle



DMA Data Transfer Interface

Pramater	Symbol	Min	Max	Units
CLK ↓→AEN ↑ Dilay time	t_{AEL}		45	ns
CLK ↑→AEN ↓ Dilay time	t_{AET}		40	ns
CLK ↑→Address floating	t_{AFAB}		90	ns
CLK ↑→Read,Write floating Dilay time	t_{AFC}		120	ns
CLK ↑→Data bus floating Dilay time	t_{AFDB}		170	ns
Read↑→Address Hold time	t_{AHR}	t_{CHY}		ns
		-100		ns
ADSTB ↑→Data Hold time	t_{AHS}	30		ns
Write ↑→Address Hold time	t_{AHW}	t_{CY}		ns
		-50		ns
CLK ↑→/DACK ↓ Dilay time	t_{AK}		170	ns
CLK ↑→/EOP↑ Dilay time	t_{AK}		170	ns
CLK ↑→/EOP↓ Dilay time	t_{AK}		170	ns
CLK ↑→Address Set time	t_{ASM}		170	ns
ADSTB ↓→Data Setup time	t_{ASS}	100		ns
CLK High level time	t_{CH}	80		ns
CLK Low level time	t_{CL}	68		ns
CLk Cycle	t_{CY}	200		ns
CLK ↑→Read,Write↓Dilay time	t_{DCL}		190	ns
CLK ↑→Read↑Dilay time	t_{DCTR}		190	ns
CLK ↑→Write ↑Dilay time	t_{DCTW}		130	ns
CLK ↑→HRQ Set time	t_{DQ}		120	ns
CLK ↑→Address Set time	t_{FAAB}		170	ns
CLK ↑→Read,Write↓ Set time	t_{FAC}		150	ns
CLK ↑→Data Set time	t_{FADB}		200	ns
CLK ↑→HLDA Setup time	t_{HS}	75		ns
/MEMR ↑→input Data Hold time	t_{IDH}	0		ns
/MEMR ↑→input Data Setup time	t_{IDS}	170		ns
/MEMW ↑→output Data Hold time	t_{ODH}	10		ns
output data set →/MEMW ↑ Set time	t_{ODV}	125		ns
CLK ↑→DREQ Setup time	t_{QS}	0		ns
CLK ↑→READY Setup time	t_{RH}	20		ns
CLK ↑→READY Hold time	t_{RS}	60		ns
CLK ↑→ADSTB ↑ Dilay time	t_{STL}		130	ns
CLK ↑→ADSTB ↓ Dilay time	t_{STT}		90	ns

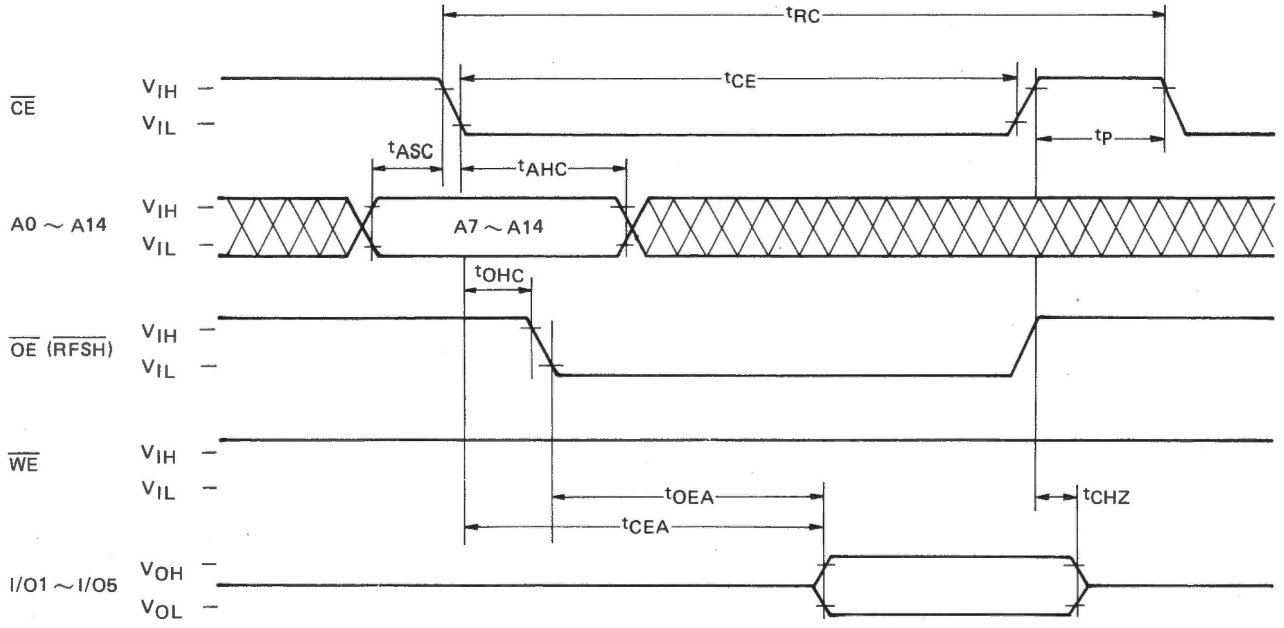
DMA DATA Transfer Interface



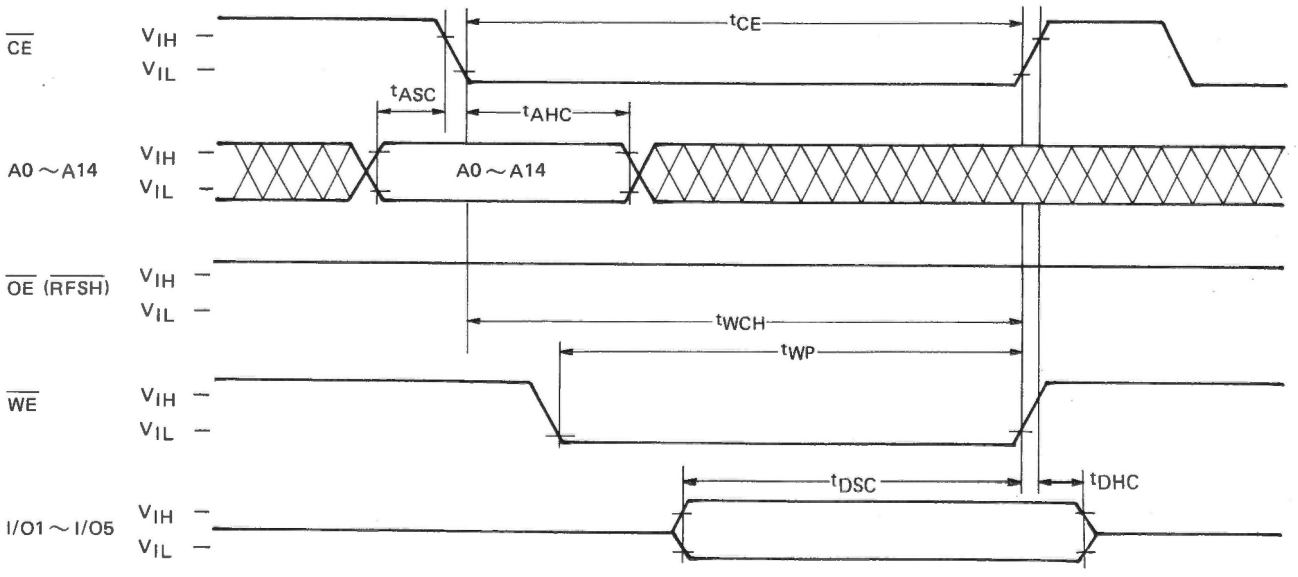
Memory Interface

Pramater	Symbol	Min	Max	Units
Random Read/Write Cycle time	t_{RC}	235		ns
/CE access time	t_{CEA}		150	ns
/OE access time	t_{OEA}		40	ns
/CE Pulse Width	t_{CE}	150	1000	ns
/CE Pre charge time	t_{P}	75		ns
/CE →Address Setup time	t_{ASC}	0		ns
/CE →Address Hold time	t_{AHC}	40		ns
/CE →/OE Hold time	t_{OHC}	0		ns
Write command Hold time	t_{WCH}	105		ns
/WE Pulse width	t_{WP}	105		ns
/CE →Input data Setup time	t_{DSC}	95		ns
/CE →Input data Hold time	t_{DHC}	0		ns
Pulse Refresh Cycle time	t_{FC}	235		ns
/CE →/RFSH Dilay time	t_{RFD}	75		ns
/RFSH Pulse width	t_{FAP}	80	1000	ns
/RFSH Precharge time	t_{FP}	30		ns
/CE →Pulse Refresh Cycle Set time	t_{FCE}	275		ns
/RFSH →/CE Dilay time	t_{FSR}	115		ns

Read Cycle



Write Cycle



LCD Interface

Pramater	Symbol	Min	Max	Units
FLM-LC Set up time	t_{FLS}	320		ns
FLM-LC Hold time	t_{FLH}	320		ns
LC High level pulse width	t_{LH}	320		ns
LC -SCK Dilay time	t_{LSD}	8		us
SCK-LC Dilay time	t_{SLD}	500		ns
Data -SCK Set up time	t_{DSS}	140		ns
Data -SCK Hold time	t_{DSH}	140		ns
LC,SCK,EWCK Rise/Fall Time	t_r, t_F		50	ns
SCK High level pulse width	t_{SH}	320		ns
SCK Low level pulse width	t_{SL}	320		ns
SCK cycle time	t_{SC}	740		ns
EWCK Set up time	t_{ES}	140		ns
EWCK Hold time	t_{EH}	140		ns
EWCK High level pulse width	t_{EWH}	140		ns
M Dilay time	t_D		50	ns